

LP2950,LP2951

LP2950/LP2951 Series of Adjustable Micropower Voltage Regulators

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Literature Number: SNVS764M

LP2950/LP2951

Series of Adjustable Micropower Voltage Regulators

General Description

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75µA typ.) and very low dropout voltage (typ. 40mV at light loads and 380mV at 100mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950-5.0 is available in the surface-mount D-Pak package, and in the popular 3-pin TO-92 package for pin-compatibility with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, LLP, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V, 3V, or 3.3V output (depending on the version), or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation

(.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

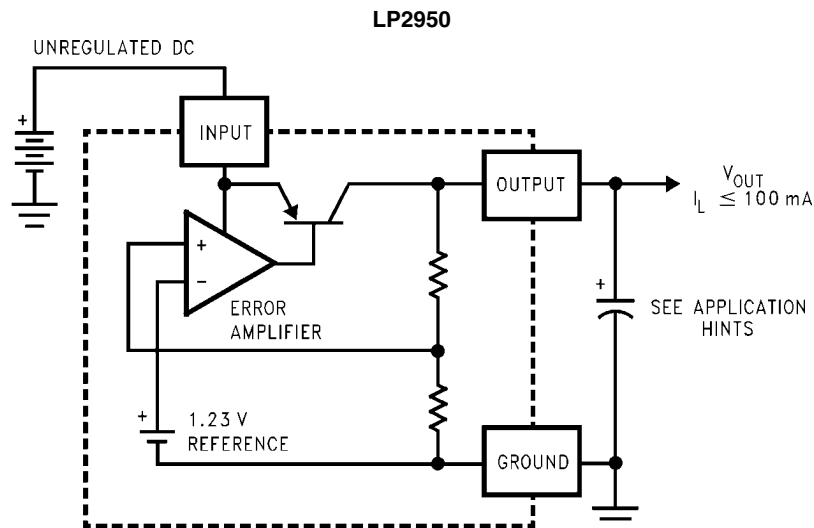
Features

- 5V, 3V, and 3.3V versions available
- High accuracy output voltage
- Guaranteed 100mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs minimum capacitance for stability
- Current and Thermal Limiting
- Stable with low-ESR output capacitors (10mΩ to 6Ω)

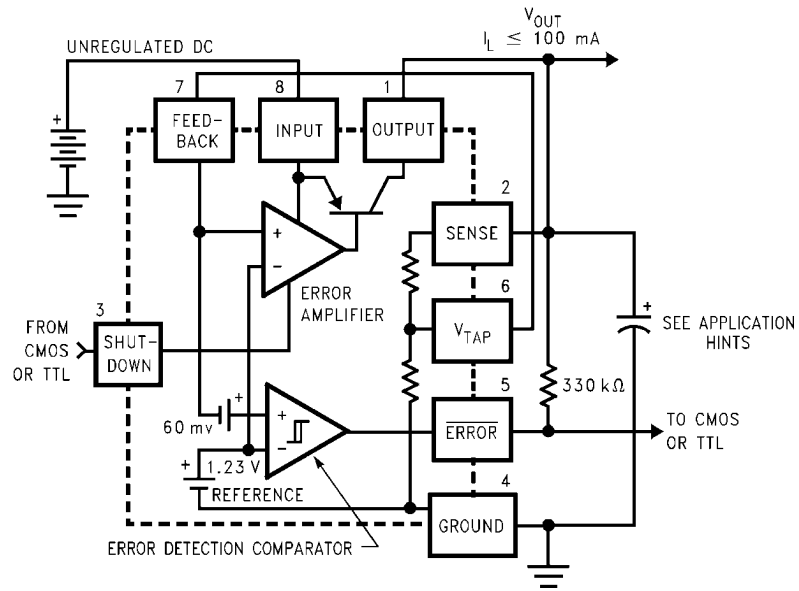
LP2951 versions only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

Block Diagram and Typical Applications



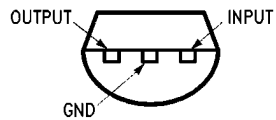
LP2951



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Connection Diagrams

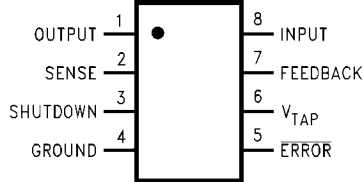
TO-92 Plastic Package (Z)



Bottom View

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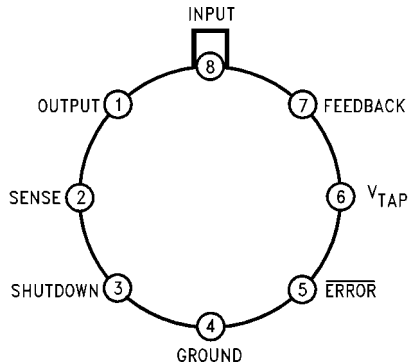
Dual-In-Line Packages (N, J) Surface-Mount Package (M, MM)



Top View

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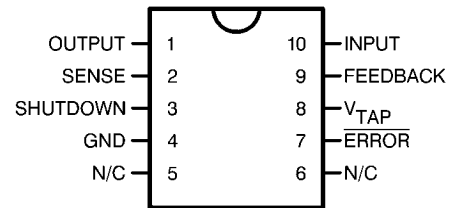
Metal Can Package (H)



Top View

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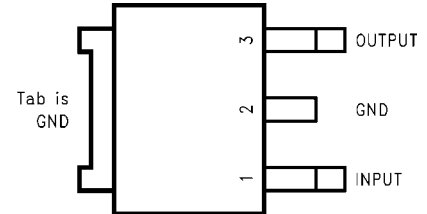
10-Lead Ceramic Surface-Mount Package (WG)



Top View

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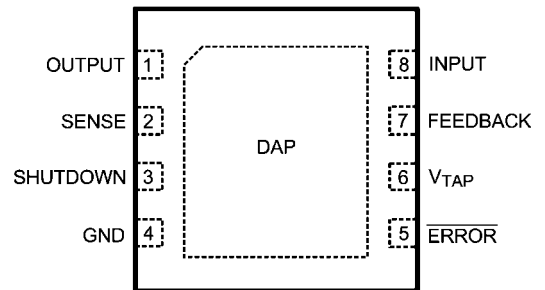
TO-252 (D-Pak)



Front View

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8-Lead LLP



Top View

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Ordering Information

Package	Temperature Range	V _{OUT}	Part Number	Package Marking	Transport Media	NSC Drawing
TO-92 (Z)	-40 < T _J < 125	3.0	LP2950ACZ-3.0	2950A CZ3.0	Bag	Z03A
			LP2950CZ-3.0	2950 CZ3.0	Bag	
		3.3	LP2950ACZ-3.3	2950A CZ3.3	Bag	
			LP2950CZ-3.3	2950 CZ3.3	Bag	
		5.0	LP2950ACZ-5.0	2950A CZ5.0	Bag	
			LP2950CZ-5.0	2950 CZ5.0	Bag	
TO-252 (D-Pak)	-40 < T _J < 125	3.0	LP2950CDT-3.0	LP2950CDT-3.0	75 Units/Rail	TD03B
			LP2950CDTX-3.0		2.5k Units Tape and Reel	
		3.3	LP2950CDT-3.3	LP2950CDT-3.3	75 Units/Rail	
			LP2950CDTX-3.3		2.5k Units Tape and Reel	
		5.0	LP2950CDT-5.0	LP2950CDT-5.0	75 Units/Rail	
			LP2950CDTX-5.0		2.5k Units Tape and Reel	
N (N-08E)	-40 < T _J < 125	3.0	LP2951ACN-3.0	LP2951ACN-3.0	40 Units/Rail	N08E
			LP2951CN-3.0	LP2951CN-3.0	40 Units/Rail	
		3.3	LP2951ACN-3.3	LP2951ACN-3.3	40 Units/Rail	
			LP2951CN-3.3	LP2951CN-3.3	40 Units/Rail	
		5.0	LP2951ACN	LP2951ACN	40 Units/Rail	
			LP2951CN	LP2951CN	40 Units/Rail	
M (M08A)	-40 < T _J < 125	3.0	LP2951ACM-3.0	2951ACM30* (where * is die rev letter)	95 Units/Rail	M08A
			LP2951ACMX-3.0		2.5k Units Tape and Reel	
			LP2951CM-3.0	2951CM30* (where * is die rev letter)	95 Units/Rail	
			LP2951CMX-3.0		2.5k Units Tape and Reel	
		3.3	LP2951ACM-3.3	2951ACM33* (where * is die rev letter)	95 Units/Rail	
			LP2951ACMX-3.3		2.5k Units Tape and Reel	
			LP2951CM-3.3	2951CM33* (where * is die rev letter)	95 Units/Rail	
			LP2951CMX-3.3		2.5k Units Tape and Reel	
		5.0	LP2951ACM	2951ACM* (where * is die rev letter)	95 Units/Rail	
			LP2951ACMX		2.5k Units Tape and Reel	
			LP2951CM	2951CM* (where * is die rev letter)	95 Units/Rail	
			LP2951CMX		2.5k Units Tape and Reel	
MM (MUA08A)	-40 < T _J < 125	3.0	LP2951ACMM-3.0	L0BA	1k Units Tape and Reel	MUA08A
			LP2951ACMMX-3.0		3.5k Units Tape and Reel	
			LP2951CMM-3.0	L0BB	1k Units Tape and Reel	
			LP2951CMMX-3.0		3.5k Units Tape and Reel	
		3.3	LP2951ACMM-3.3	L0CA	1k Units Tape and Reel	
			LP2951ACMMX-3.3		3.5k Units Tape and Reel	
			LP2951CMM-3.3	L0CB	1k Units Tape and Reel	
			LP2951CMMX-3.3		3.5k Units Tape and Reel	
		5.0	LP2951ACMM	L0DA	1k Units Tape and Reel	
			LP2951ACMMX		3.5k Units Tape and Reel	
			LP2951CMM	L0DB	1k Units Tape and Reel	
			LP2951CMMX		3.5k Units Tape and Reel	
J (J08A)	-55 < T _J < 150	5.0	LP2951J/883	See MIL/AERO Datasheet	40 Units/Rail	J08A
H (H08C)	-55 < T _J < 150	5.0	LP2951H/883	See MIL/AERO Datasheet	Tray	H08C
WG (WG10A)	-55 < T _J < 150	5.0	LP2951WG/883	See MIL/AERO Datasheet	Tray	WG10A

Package	Temperature Range	V _{OUT}	Part Number	Package Marking	Transport Media	NSC Drawing
8-lead LLP	$-40 < T_J < 125$	3.0	LP2951ACSD-3.0	51AC30	1k Units Tape and Reel	SDC08A
			LP2951ACSDX-3.0		4.5k Units Tape and Reel	
			LP2951CSD-3.0	51AC30B	1k Units Tape and Reel	
			LP2951CSDX-3.0		4.5k Units Tape and Reel	
		3.3	LP2951ACSD-3.3	51AC33	1k Units Tape and Reel	
			LP2951ACSDX-3.3		4.5k Units Tape and Reel	
			LP2951CSD-3.3	51AC33B	1k Units Tape and Reel	
			LP2951CSDX-3.3		4.5k Units Tape and Reel	
		5.0	LP2951ACSD	2951AC	1k Units Tape and Reel	
			LP2951ACSDX		4.5k Units Tape and Reel	
			LP2951CSD	2951ACB	1k Units Tape and Reel	
			LP2951CSDX		4.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Supply Voltage	−0.3 to +30V
SHUTDOWN Input Voltage, Error Comparator Output Voltage, (Note 9)	
FEEDBACK Input Voltage (Note 9, Note 10)	−1.5 to +30V
Power Dissipation	Internally Limited
Junction Temperature (T_J)	+150°C
Ambient Storage Temperature	−65° to +150°C
Soldering Dwell Time, Temperature	
Wave	4 seconds, 260°C
Infrared	10 seconds, 240°C
Vapor Phase	75 seconds, 219°C

ESD Rating

Human Body Model (Note 18)

2500V

Operating Ratings (Note 1)

Maximum Input Supply Voltage	30V
Junction Temperature Range (T_J) (Note 8)	
LP2950AC-XX, LP2950C-XX	−40° to +125°C
LP2951	−55° to +150°C
LP2951AC-XX, LP2951C-XX	−40° to +125°C

Electrical Characteristics (Note 2)

Parameter	Conditions (<i>Note 2</i>)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (<i>Note 3</i>) (<i>Note 16</i>)	Typ	Tested Limit (<i>Note 3</i>)	Design Limit (<i>Note 4</i>)	Typ	Tested Limit (<i>Note 3</i>)	Design Limit (<i>Note 4</i>)	
3V Versions (<i>Note 17</i>)										
Output Voltage	T _J = 25°C	3.0	3.015 2.985	3.0	3.015 2.985		3.0	3.030 2.970		V max V min
	–25°C ≤ T _J ≤ 85°C	3.0		3.0		3.030 2.970	3.0		3.045 2.955	V max V min
	Full Operating Temperature Range	3.0	3.036 2.964	3.0		3.036 2.964	3.0		3.060 2.940	V max V min
Output Voltage	100μA ≤ I _L ≤ 100mA	3.0	3.045	3.0		3.042	3.0		3.072	V max
	T _J ≤ T _{JMAX}		2.955			2.958			2.928	V min
3.3V Versions (<i>Note 17</i>)										
Output Voltage	T _J = 25°C	3.3	3.317 3.284	3.3	3.317 3.284		3.3	3.333 3.267		V max V min
	–25°C ≤ T _J ≤ 85°C	3.3		3.3		3.333 3.267	3.3		3.350 3.251	V max V min
	Full Operating Temperature Range	3.3	3.340 3.260	3.3		3.340 3.260	3.3		3.366 3.234	V max V min
Output Voltage	100μA ≤ I _L ≤ 100mA	3.3	3.350	3.3		3.346	3.3		3.379	V max
	T _J ≤ T _{JMAX}		3.251			3.254			3.221	V min
5V Versions (<i>Note 17</i>)										
Output Voltage	T _J = 25°C	5.0	5.025 4.975	5.0	5.025 4.975		5.0	5.05 4.95		V max V min
	–25°C ≤ T _J ≤ 85°C	5.0		5.0		5.05 4.95	5.0		5.075 4.925	V max V min
	Full Operating Temperature Range	5.0	5.06 4.94	5.0		5.06 4.94	5.0		5.1 4.9	V max V min
Output Voltage	100μA ≤ I _L ≤ 100mA	5.0	5.075	5.0		5.075	5.0		5.12	V max
	T _J ≤ T _{JMAX}		4.925			4.925			4.88	V min

Parameter	Conditions (<i>Note 2</i>)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (<i>Note 3</i>) (<i>Note 16</i>)	Typ	Tested Limit (<i>Note 3</i>)	Design Limit (<i>Note 4</i>)	Typ	Tested Limit (<i>Note 3</i>)	Design Limit (<i>Note 4</i>)	
All Voltage Options										
Output Voltage Temperature Coefficient	(<i>Note 12</i>)	20	120	20		100	50		150	ppm/°C
Line Regulation (<i>Note 14</i>)	(V _O NOM + 1)V ≤ V _{in} ≤ 30V (<i>Note 15</i>)	0.03	0.1 0.5	0.03	0.1	0.2	0.04	0.2	0.4	% max % max
Load Regulation (<i>Note 14</i>)	100μA ≤ I _L ≤ 100mA	0.04	0.1 0.3	0.04	0.1	0.2	0.1	0.2	0.3	% max % max
Dropout Voltage (<i>Note 5</i>)	I _L = 100μA	50	80 150	50	80	150	50	80	150	mV max mV max
	I _L = 100mA	380	450 600	380	450	600	380	450	600	mV max mV max
Ground Current	I _L = 100μA	75	120 140	75	120	140	75	120	140	μA max μA max
	I _L = 100mA	8	12 14	8	12	14	8	12	14	mA max mA max
Dropout	V _{in} = (V _O NOM – 0.5) V	110	170	110	170		110	170		μA max
Ground Current	I _L = 100μA		200			200			200	μA max
Current Limit	V _{out} = 0	160	200 220	160	200	220	160	200	220	mA max mA max
Thermal Regulation	(<i>Note 13</i>)	0.05	0.2	0.05	0.2		0.05	0.2		%/W max
Output Noise, 10 Hz to 100 kHz	C _L = 1μF (5V Only)	430		430			430			μV rms
	C _L = 200μF	160		160			160			μV rms
	C _L = 3.3μF (Bypass = 0.01μF Pins 7 to 1 (LP2951))	100		100			100			μV rms
8-pin Versions Only		LP2951		LP2951AC-XX			LP2951C-XX			
Reference		1.23 5	1.25	1.23 5	1.25		1.23 5	1.26		V max
Voltage			1.26 1.22 1.2		1.22	1.26 1.2		1.21	1.27 1.2	V max V min V min
	(<i>Note 7</i>)		1.27 1.19			1.27 1.19			1.285 1.185	V max V min
Feedback Pin Bias Current		20	40 60	20	40	60	20	40	60	nA max nA max
Reference Voltage Temperature Coefficient	(<i>Note 12</i>)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C

Parameter	Conditions (<i>Note 2</i>)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (<i>Note 3</i>) (<i>Note 16</i>)	Typ	Tested Limit (<i>Note 3</i>)	Design Limit (<i>Note 4</i>)	Typ	Tested Limit (<i>Note 3</i>)	Design Limit (<i>Note 4</i>)	
Error Comparator										
Output Leakage Current	V _{OH} = 30V	0.01	1 2	0.01	1	2	0.01	1	2	μA max μA max
Output Low Voltage	V _{in} = (V _O NOM – 0.5) V I _{OL} = 400μA	150	250 400	150	250	400	150	250	400	mV max mV max
Upper Threshold Voltage	(<i>Note 6</i>)	60	40 25	60	40	25	60	40	25	mV min mV min
Lower Threshold Voltage	(<i>Note 6</i>)	75	95 140	75	95	140	75	95	140	mV max mV max
Hysteresis	(<i>Note 6</i>)	15		15			15			mV
Shutdown Input										
Input Logic Voltage	Low (Regulator ON) High (Regulator OFF)	1.3	0.6 2.0	1.3		0.7 2.0	1.3		0.7 2.0	V V max V min
Shutdown Pin Input Current	V _{shutdown} = 2.4V	30	50 100	30	50	100	30	50	100	μA max μA max
	V _{shutdown} = 30V	450	600 750	450	600	750	450	600	750	μA max μA max
Regulator Output Current in Shutdown	(<i>Note 11</i>)	3	10 20	3	10	20	3	10	20	μA max μA max

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: Unless otherwise specified all limits guaranteed for $V_{IN} = (V_{ONOM} + 1)V$, $I_L = 100\mu A$ and $C_L = 1\mu F$ for 5V versions and $2.2\mu F$ for 3V and 3.3V versions. Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for $T_A = T_J = 25^\circ C$. Additional conditions for the 8-pin versions are FEEDBACK tied to V_{TAP} , OUTPUT tied to SENSE, and $V_{SHUTDOWN} \leq 0.8V$.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at $V_{in} = (V_{ONOM} + 1)V$. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain $= V_{out}/V_{ref} = (R1 + R2)/R2$. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by $95mV \times 5V/1.235V = 384 mV$. Thresholds remain constant as a percent of V_{out} as V_{out} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: $V_{ref} \leq V_{out} \leq (V_{in} - 1V)$, $2.3V \leq V_{in} \leq 30V$, $100\mu A \leq I_L \leq 100mA$, $T_J \leq T_{JMAX}$.

Note 8: The junction-to-ambient thermal resistances are as follows: $180^\circ C/W$ and $160^\circ C/W$ for the TO-92 package with 0.40 inch and 0.25 inch leads to the printed circuit board (PCB) respectively, $105^\circ C/W$ for the molded plastic DIP (N), $130^\circ C/W$ for the ceramic DIP (J), $160^\circ C/W$ for the molded plastic SOP (M), $200^\circ C/W$ for the molded plastic MSOP (MM), and $160^\circ C/W$ for the metal can package (H). The above thermal resistances for the N, J, M, and MM packages apply when the package is soldered directly to the PCB. Junction-to-case thermal resistance for the H package is $20^\circ C/W$. Junction-to-case thermal resistance for the TO-252 package is $5.4^\circ C/W$. The value of θ_{JA} for the LLP package is typically $51^\circ C/W$ but is dependent on the PCB trace area, trace material, and the number of layers and thermal vias. For details of thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187.

Note 9: May exceed input supply voltage.

Note 10: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 11: $V_{shutdown} \geq 2V$, $V_{in} \leq 30V$, $V_{out} = 0$, Feedback pin tied to V_{TAP} .

Note 12: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 13: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50mA load pulse at $V_{IN} = 30V$ (1.25W pulse) for $T = 10ms$.

Note 14: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

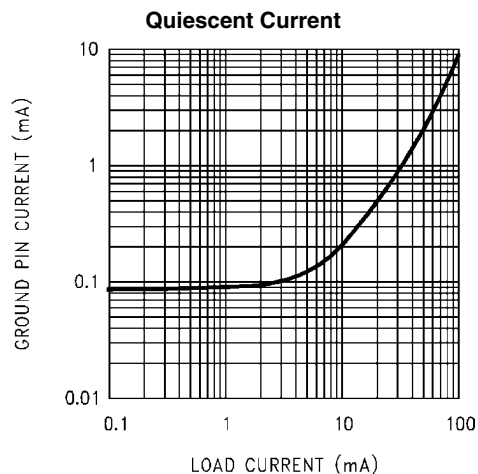
Note 15: Line regulation for the LP2951 is tested at $150^\circ C$ for $I_L = 1mA$. For $I_L = 100\mu A$ and $T_J = 125^\circ C$, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Note 16: A Military RETS specification is available on request. At time of printing, the LP2951 RETS specification complied with the boldface limits in this column. The LP2951H, WG, or J may also be procured as Standard Military Drawing Spec #5962-3870501MGA, MXA, or MPA.

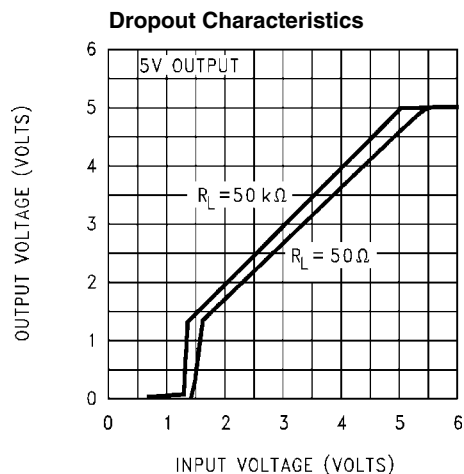
Note 17: All LP2950 devices have the nominal output voltage coded as the last two digits of the part number. In the LP2951 products, the 3.0V and 3.3V versions are designated by the last two digits, but the 5V version is denoted with no code at this location of the part number (refer to ordering information table).

Note 18: Human Body Model (HBM) is 1.5k Ω in series with 100pF; LP2950 passes 2.5 kV(HBM) ESD; LP2951 passes 2.5 kV(HBM) except: Feedback pin passes 1kV(HBM) and Shutdown pin passes 2kV(HBM).

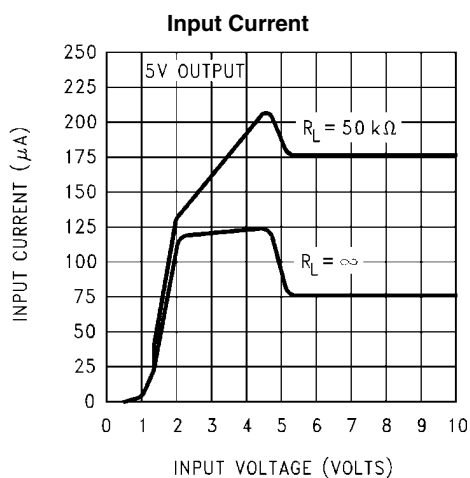
Typical Performance Characteristics



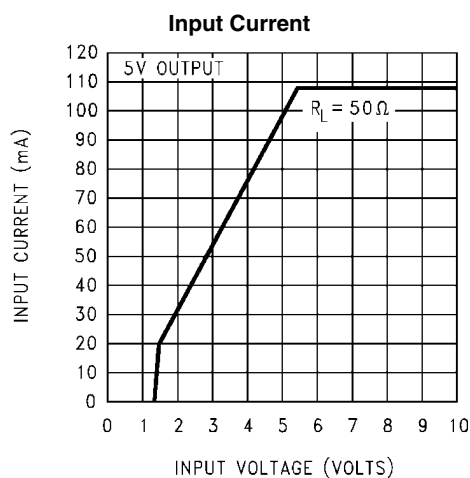
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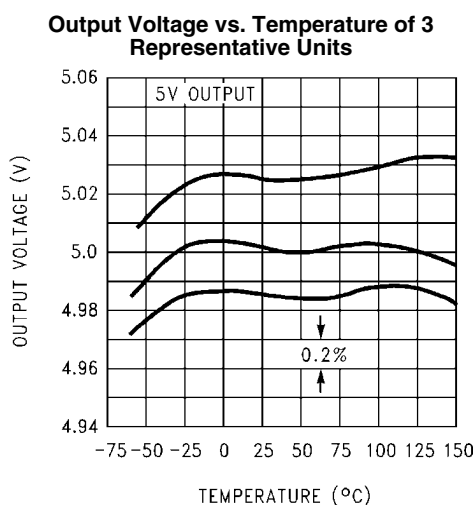
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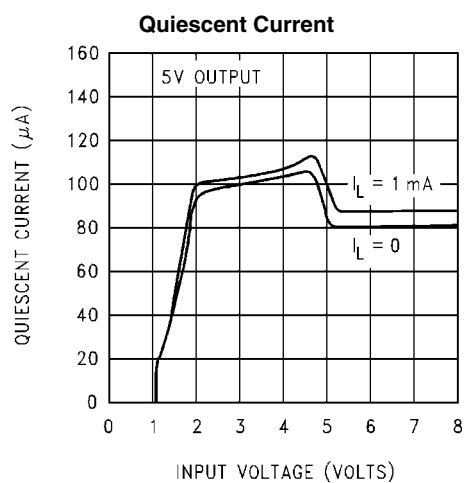
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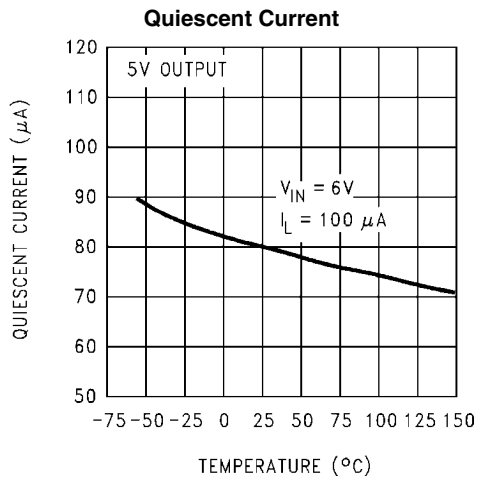
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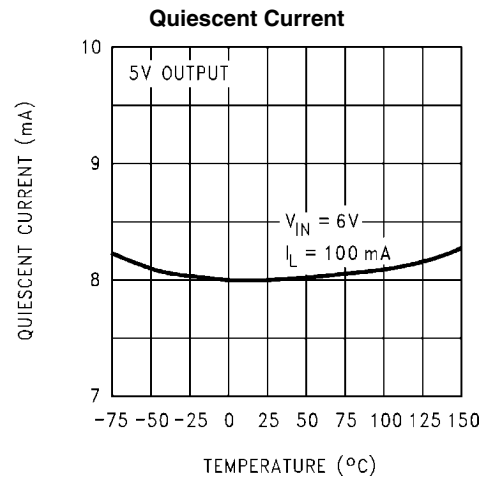
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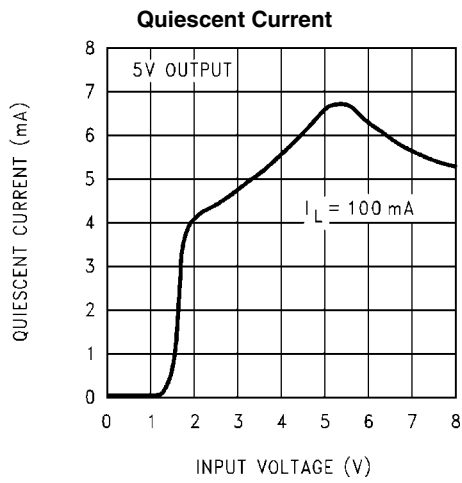
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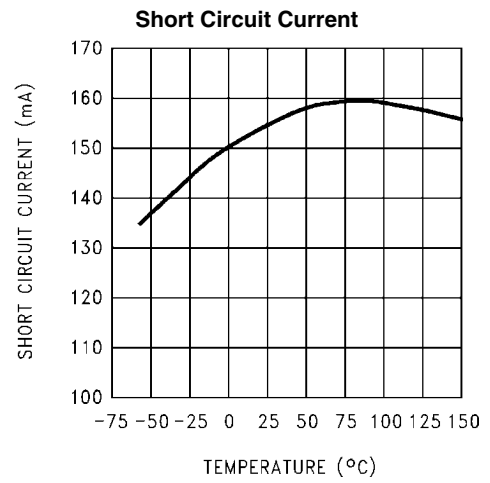
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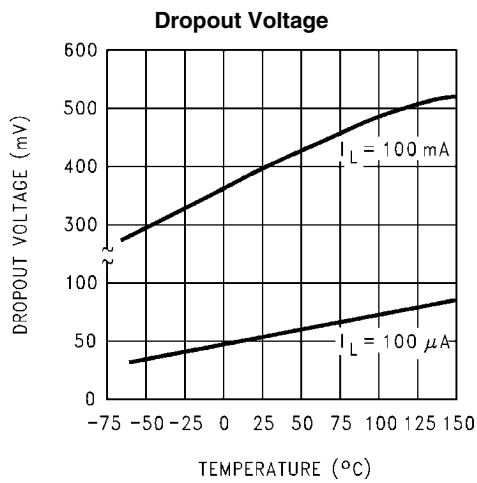
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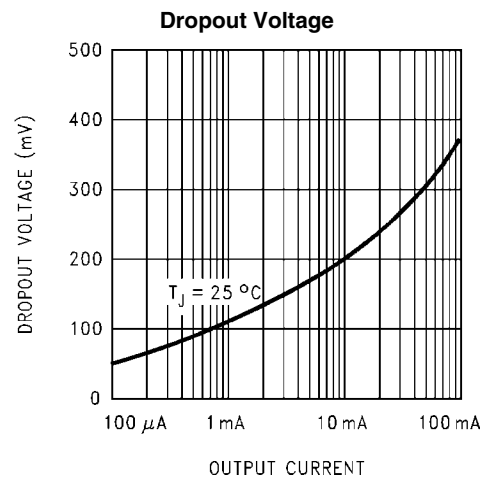
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854636

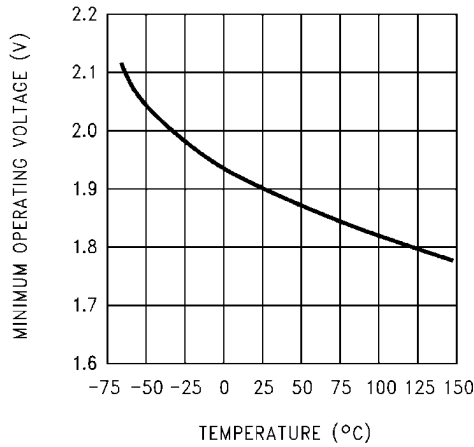


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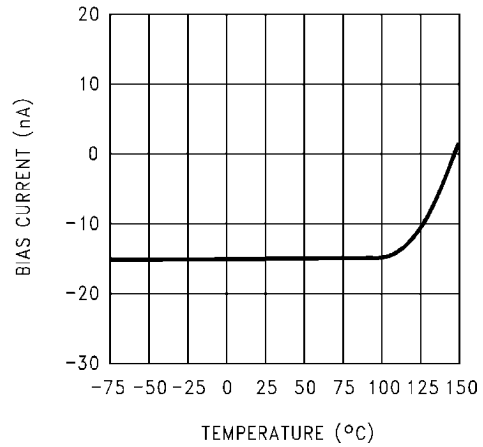
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LP2951 Minimum Operating Voltage



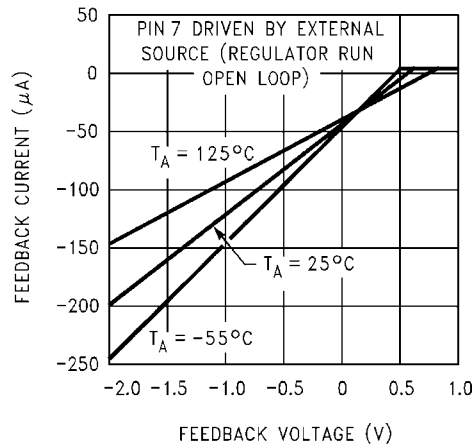
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LP2951 Feedback Bias Current



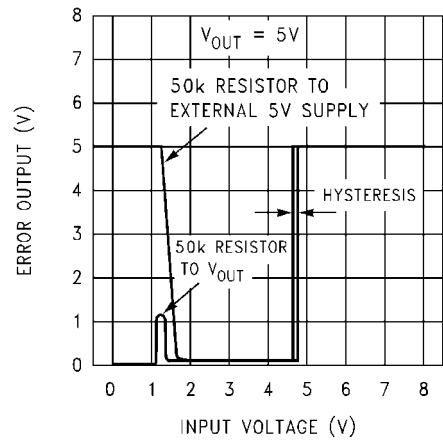
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LP2951 Feedback Pin Current



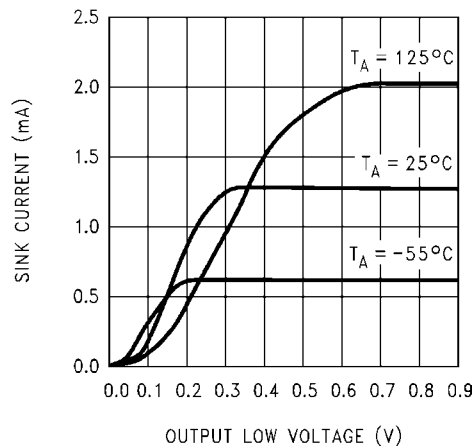
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LP2951 Error Comparator Output



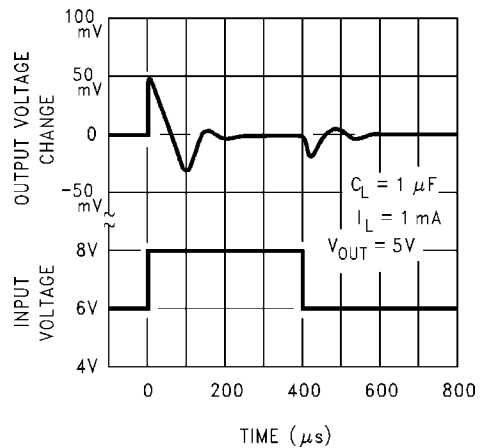
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LP2951 Comparator Sink Current

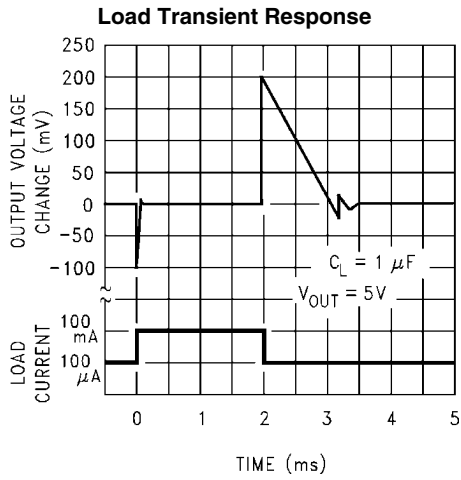


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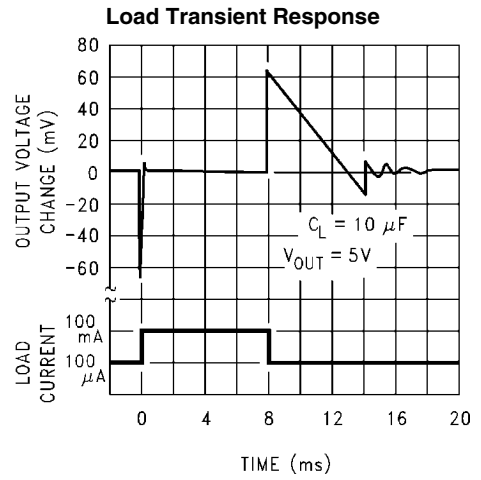
Line Transient Response



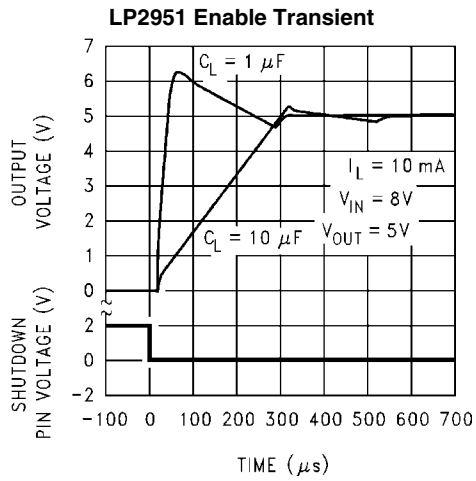
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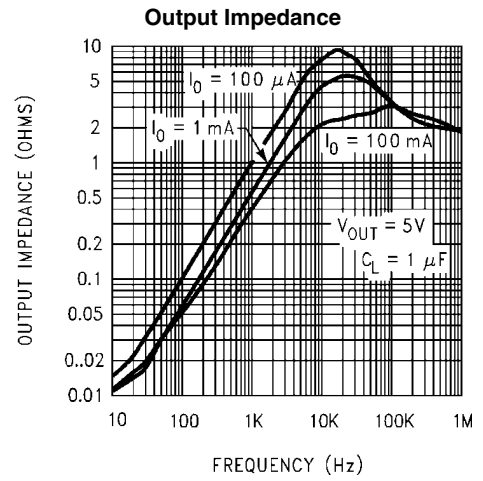
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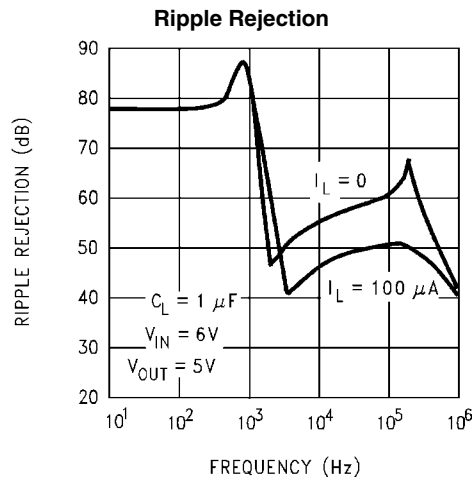
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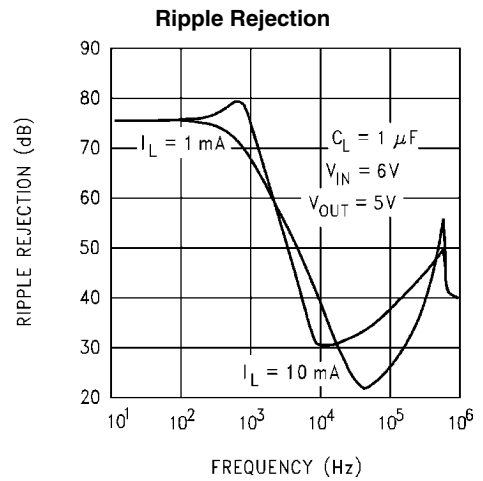
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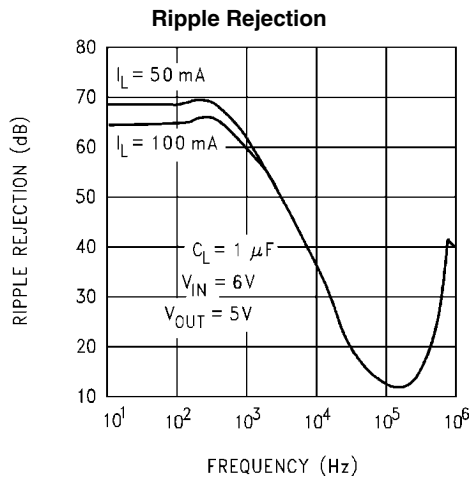
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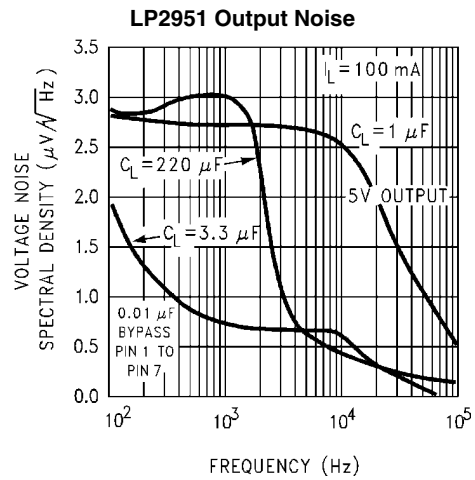
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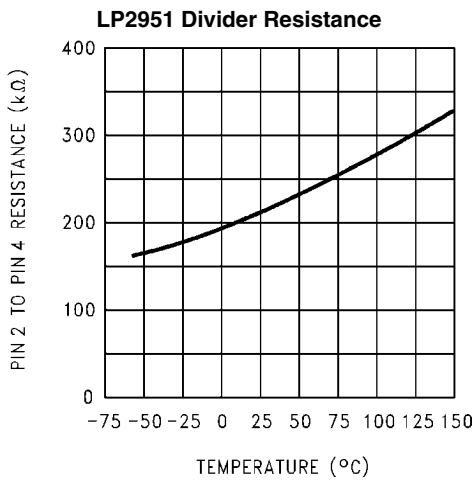
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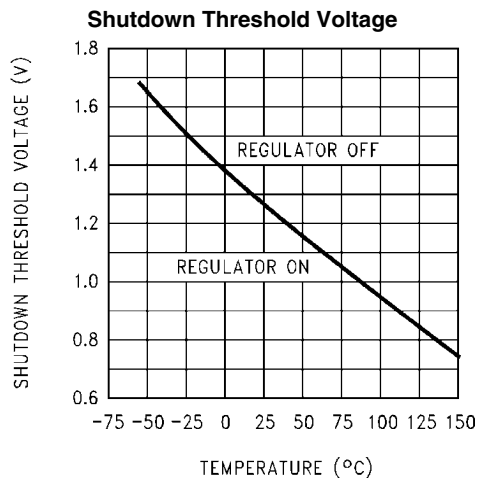
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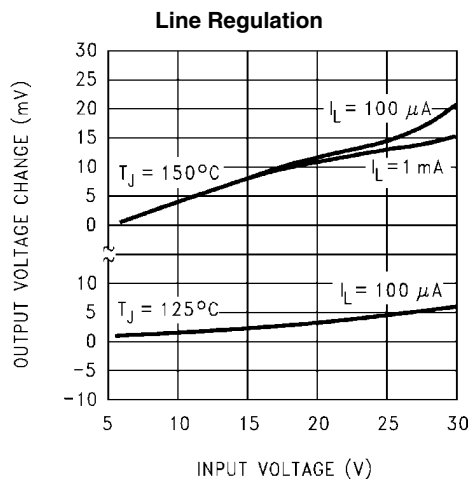
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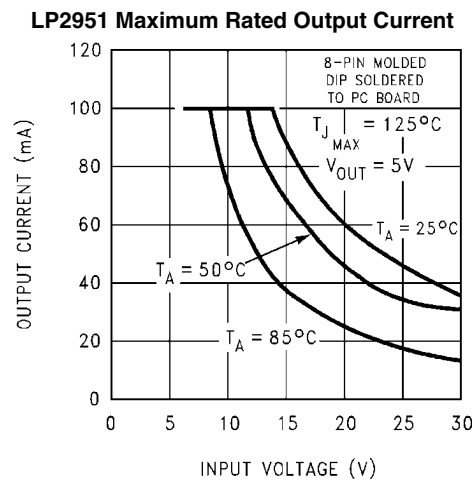
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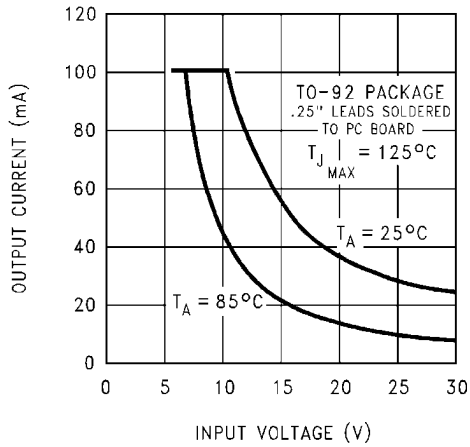


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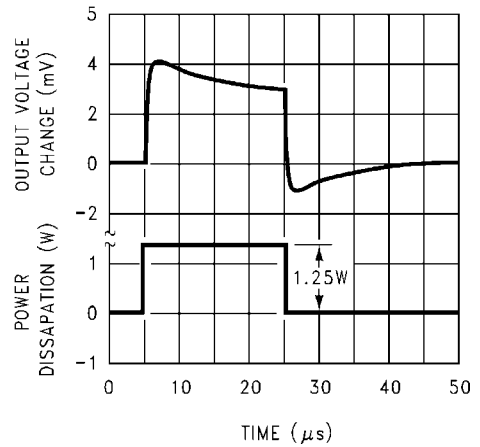
854656

LP2950 Maximum Rated Output Current



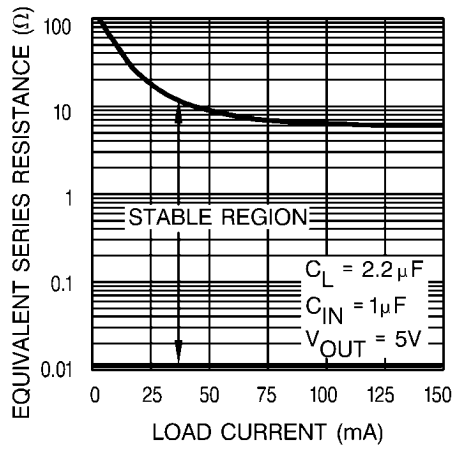
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Thermal Response



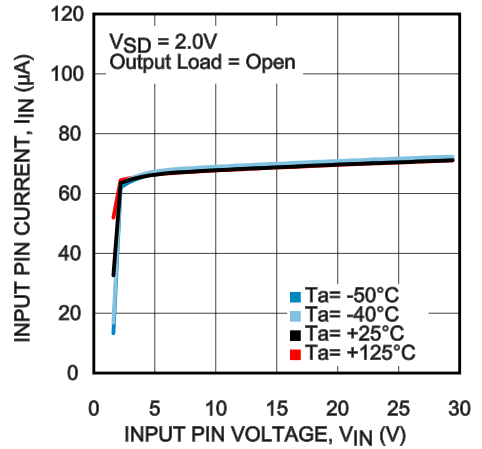
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Output Capacitor ESR Range



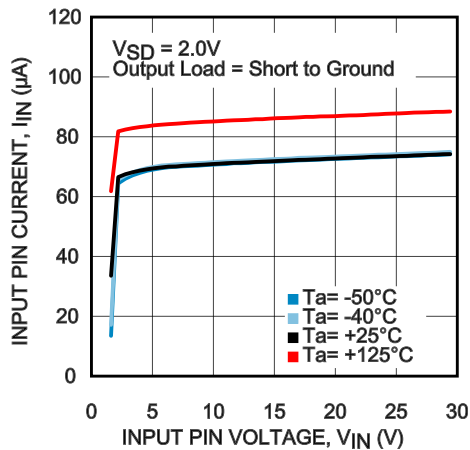
854663

LP2951 Input Pin Current vs Input Voltage



854672

LP2951 Input Pin Current vs Input Voltage

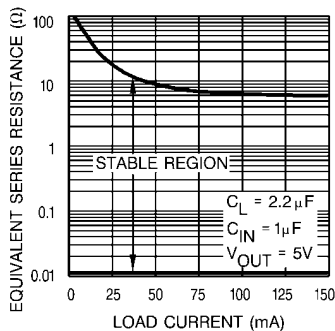


854673

Application Hints

OUTPUT CAPACITOR REQUIREMENTS

A 1.0 μF (or greater) capacitor is required between the output and ground for stability at output voltages of 5V or higher. At lower output voltages, more capacitance is required (2.2 μF or more is recommended for 3.0V and 3.3V versions). Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytic work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about -30°C , so solid tantalums are recommended for operation below -25°C . The important parameters of the capacitor are an ESR of about 5Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.



854663

FIGURE 1. Output Capacitor ESR Range

The reason for the lower ESR limit is that the loop compensation of the feedback loop relies on the capacitance value and the ESR value of the output capacitor to provide the zero that gives added phase lead (See [Figure 1](#)).

$$f_z = (1 / (2 \times \pi \times C_{OUT} \times \text{ESR}))$$

Using the 2.2 μF value from the *Output Capacitor ESR Range* curve ([Figure 1](#)), a useful range for f_z can be estimated:

$$f_{z(\text{MIN})} = (1 / (2 \times \pi \times 2.2 \mu\text{F} \times 5\Omega)) = 14.5 \text{ kHz}$$

$$f_{z(\text{MAX})} = (1 / (2 \times \pi \times 2.2 \mu\text{F} \times 0.05\Omega)) = 318 \text{ kHz}$$

For ceramic capacitors, the low ESR produces a zero at a frequency that is too high to be useful, so meaningful phase lead does not occur. A ceramic output capacitor can be used if a series resistance is added (recommended value of resistance about 0.1Ω to 2Ω) to simulate the needed ESR. Only X5R, X7R, or better, MLCC types should be used, and should have a DC voltage rating at least twice the $V_{OUT(\text{NOM})}$ value.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 μF for currents below 10 mA or 0.1 μF for currents below 1 mA. Using the adjustable versions at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100mA load at 1.23V output (Output shorted to Feedback) a 3.3 μF (or greater) capacitor should be used.

Unlike many other regulators, the LP2950 will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951

versions with external resistors, a minimum load of 1 μA is recommended.

Applications having conditions that may drive the LP2950/51 into nonlinear operation require special consideration. Nonlinear operation will occur when the output voltage is held low enough to force the output stage into output current limiting while trying to pull the output voltage up to the regulated value. The internal loop response time will control how long it takes for the device to regain linear operation when the output has returned to the normal operating range. There are three significant nonlinear conditions that need to be considered, all can force the output stage into output current limiting mode, all can cause the output voltage to over-shoot with low value output capacitors when the condition is removed, and the recommended generic solution is to set the output capacitor to a value not less than 10 μF . Although the 10 μF value for C_{OUT} may not eliminate the output voltage over-shoot in all cases, it should lower it to acceptable levels ($<10\%$ of $V_{OUT(\text{NOM})}$) in the majority of cases. In all three of these conditions, applications with lighter load currents are more susceptible to output voltage over-shoot than applications with higher load currents.

- 1) At power-up, with the input voltage rising faster than output stage can charge the output capacitor.

$$V_{IN} t_{\text{RISE}(\text{MIN})} > ((C_{OUT} / 100 \text{ mA}) \times \Delta V_{IN})$$

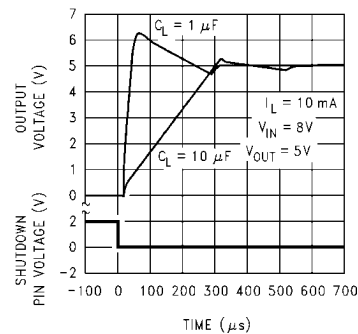
Where $\Delta V_{IN} = V_{OUT(\text{NOM})} + 1.0\text{V}$

- 2) Recovery from an output short circuit to ground condition.

$$C_{OUT(\text{MIN})} \approx (160 \text{ mA} - I_{\text{LOAD}(\text{NOM})}) / ((V_{OUT(\text{NOM})} / 10) / 25 \mu\text{s})$$

- 3) Toggling the LP2951 SHUTDOWN pin from high (i.e. OFF) to low (i.e. ON).

$$C_{OUT(\text{MIN})} \approx (160 \text{ mA} - I_{\text{LOAD}(\text{NOM})}) / ((V_{OUT(\text{NOM})} / 10) / 25 \mu\text{s})$$



854647

FIGURE 2. LP2951 Enable Transient

INPUT CAPACITOR REQUIREMENTS

A minimum 1 μF tantalum, ceramic or aluminum electrolytic capacitor should be placed from the LP2950/LP2951 input pin to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

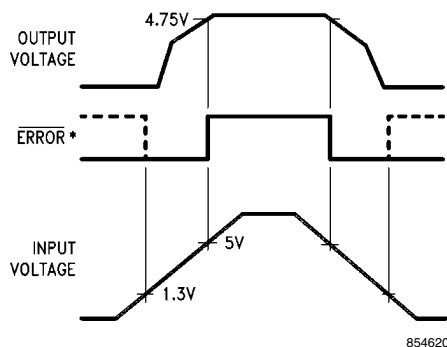
ERROR DETECTION COMPARATOR OUTPUT

The comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60mV divided by the 1.235 reference voltage. (Refer to

the block diagram in the front of the datasheet.) This trip level remains “5% below normal” regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 3 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. For 5V versions, the $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which $V_{\text{OUT}} = 4.75\text{V}$). Since the LP2951's dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pull up resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 μA , this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 M Ω . The resistor is not required if this output is unused.



*When $V_{\text{IN}} \leq 1.3\text{V}$, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see Figure 4), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10k Ω suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

FIGURE 3. $\overline{\text{ERROR}}$ Output Timing

PROGRAMMING THE OUTPUT VOLTAGE (LP2951)

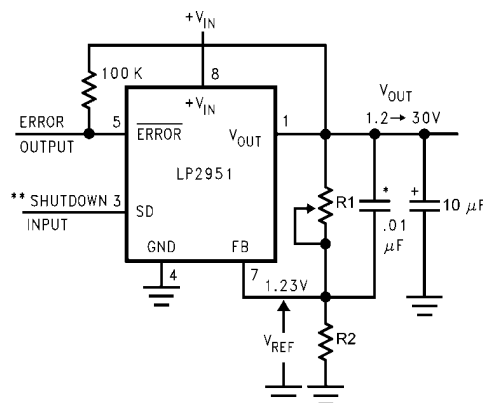
The LP2951 may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying the output and sense pins together, and also tying the feedback and V_{TAP} pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in Figure 4, an external pair of resistors is required.

The complete equation for the output voltage is

$$V_{\text{OUT}} = V_{\text{REF}} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{\text{FB}} R_1$$

where V_{REF} is the nominal 1.235V reference voltage and I_{FB} is the feedback pin bias current, nominally -20nA. The minimum recommended load current of 1 μA forces an upper limit of 1.2 M Ω on the value of R_2 , if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will

produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1 . For better accuracy, choosing $R_2 = 100\text{ k}\Omega$ reduces this error to 0.17% while increasing the resistor program current to 12 μA . Since the LP2951 typically draws 60 μA at no load with Pin 2 open-circuited, this is a small price to pay.



*See Application Hints

$$V_{\text{out}} = V_{\text{Ref}} \left(1 + \frac{R_1}{R_2}\right)$$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

FIGURE 4. Adjustable Regulator

Stray capacitance to the LP2951 Feedback terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between the Output pin and the Feedback pin, and increasing the output capacitor to at least 3.3 μF , will fix this problem.

REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP2950 but is relatively inefficient, as increasing the capacitor from 1 μF to 220 μF only decreases the noise from 430 $\mu\text{V}_{\text{(RMS)}}$ to 160 $\mu\text{V}_{\text{(RMS)}}$ for a 100 kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1 , since it reduces the high frequency gain from 4 to unity. Pick

$$C_{\text{BYPASS}} \cong \frac{1}{2\pi R_1 \cdot 200\text{ Hz}}$$

or about 0.01 μF . When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 100 μV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

LLP MOUNTING

The SDC08A (No Pullback) 8-Lead LLP package requires specific mounting techniques which are detailed in National Semiconductor Application Note # 1187. Referring to the section **PCB Design Recommendations** in AN-1187 (Page 5), it should be noted that the pad style which should be used with the LLP package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The thermal dissipation of the LLP package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

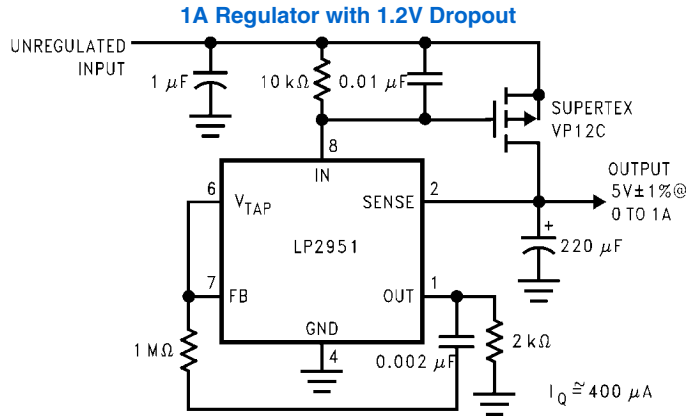
The DAP (exposed pad) on the bottom of the LLP package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the eight pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device lead 4 (i.e. GND). Alternately, but not recommended, the DAP may be left floating (i.e. no electrical

connection). The DAP must not be connected to any potential other than ground.

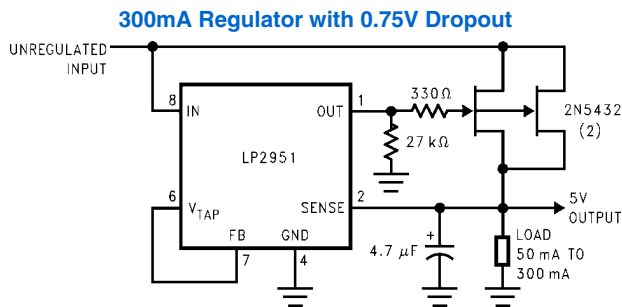
For the LP2951 in the SDC08A 8-Lead LLP package, the junction-to-case thermal rating, θ_{JC} , is 14.2°C/W, where the case is the bottom of the package at the center of the DAP. The junction-to-ambient thermal performance for the LP2951 in the SDC08A 8-Lead LLP package, using the JEDEC JESD51 standards is summarized in the following table:

Board Type	Thermal Vias	θ_{JC}	θ_{JA}
JEDEC 2-Layer JESD 51-3	None	14.2°C/W	185°C/W
JEDEC 4-Layer JESD 51-7	1	14.2°C/W	68°C/W
	2	14.2°C/W	60°C/W
	4	14.2°C/W	51°C/W
	6	14.2°C/W	48°C/W

Typical Applications

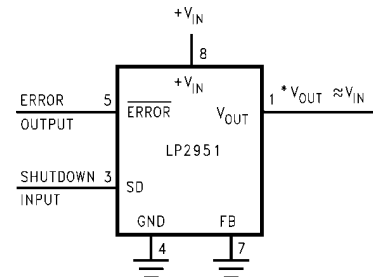


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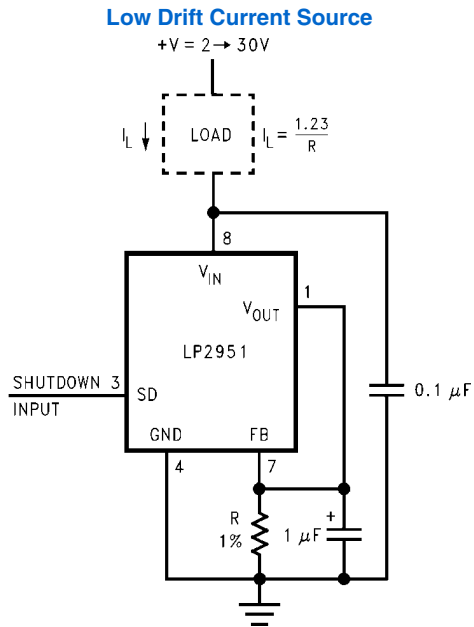
854621

Wide Input Voltage Range Current Limiter



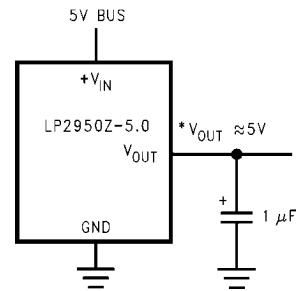
854609

*Minimum input-output voltage ranges from 40mV to 400mV, depending on load current. Current limit is typically 160mA.



854608

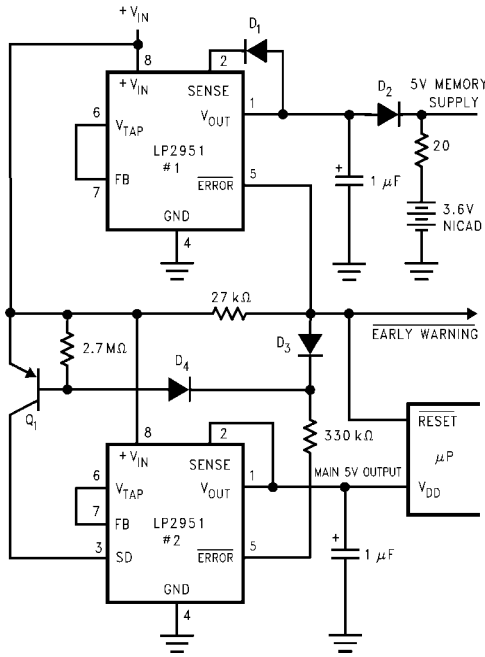
5 Volt Current Limiter



854610

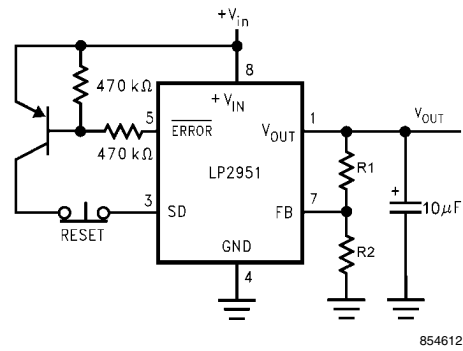
*Minimum input-output voltage ranges from 40mV to 400mV, depending on load current. Current limit is typically 160mA.

Regulator with Early Warning and Auxiliary Output



854611

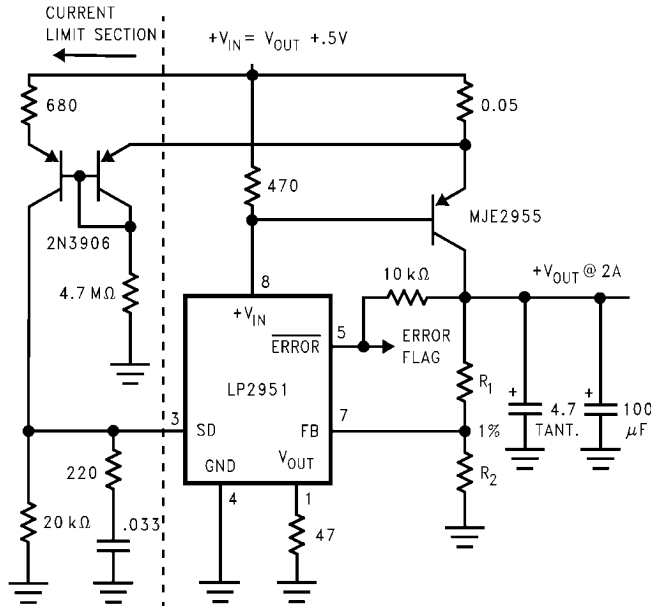
Latch Off When Error Flag Occurs



854612

- Early warning flag on low input voltage
- Main output latches off at lower input voltages
- Battery backup on auxiliary output
- Operation: Reg. #1's V_{OUT} is programmed one diode drop above 5V. Its error flag becomes active when $V_{IN} \leq 5.7V$. When V_{IN} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When V_{IN} again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

2 Ampere Low Dropout Regulator

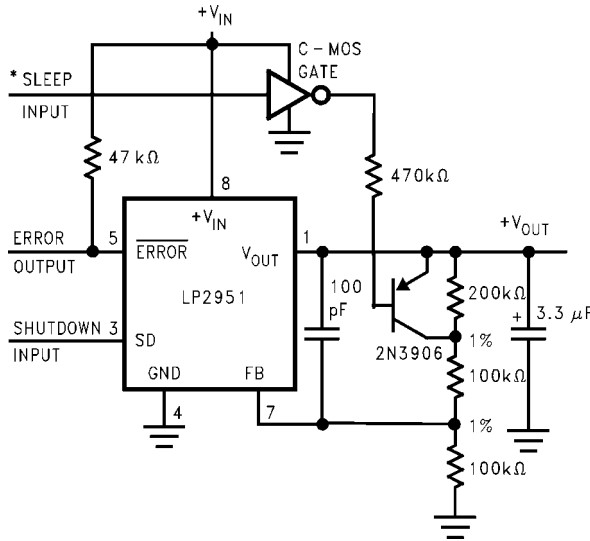


854613

$$V_{out} = 1.23V \left(1 + \frac{R_1}{R_2} \right)$$

For 5V_{out}, use internal resistors. Wire pin 6 to 7, & wire pin 2 to +V_{out} Bus.

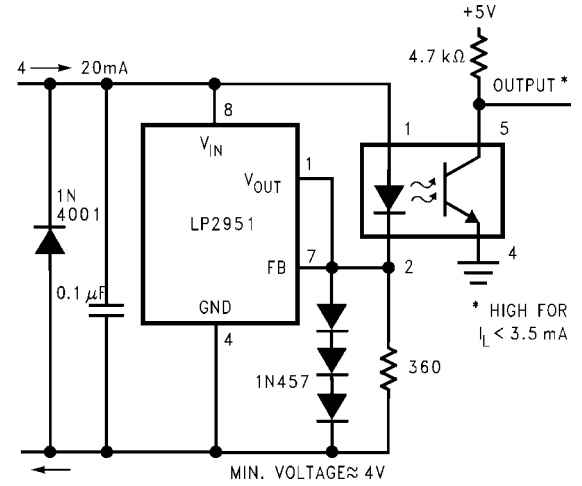
5V Regulator with 2.5V Sleep Function



854614

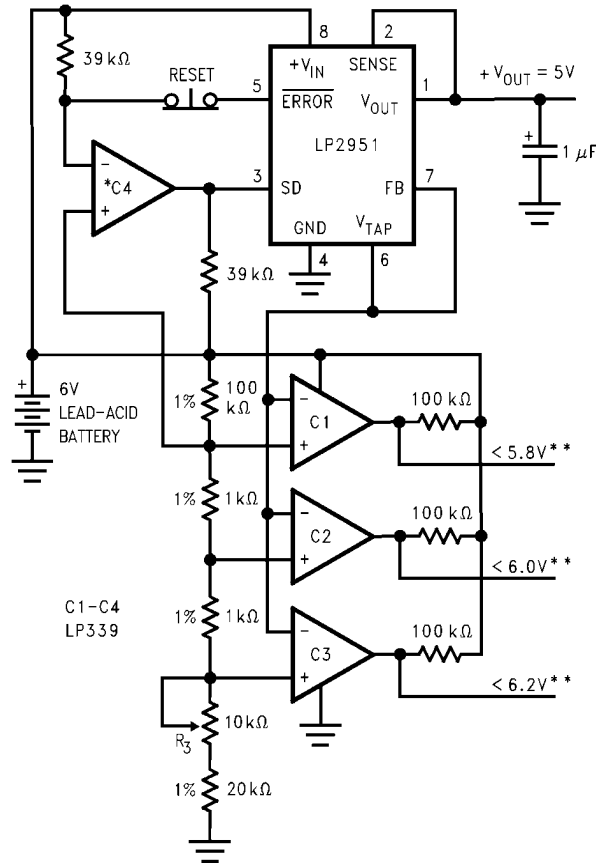
*High input lowers V_{out} to 2.5V

Open Circuit Detector for 4 → 20mA Current Loop



854615

Regulator with State-of-Charge Indicator



854616

*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V.

**Outputs go low when V_{in} drops below designated thresholds.

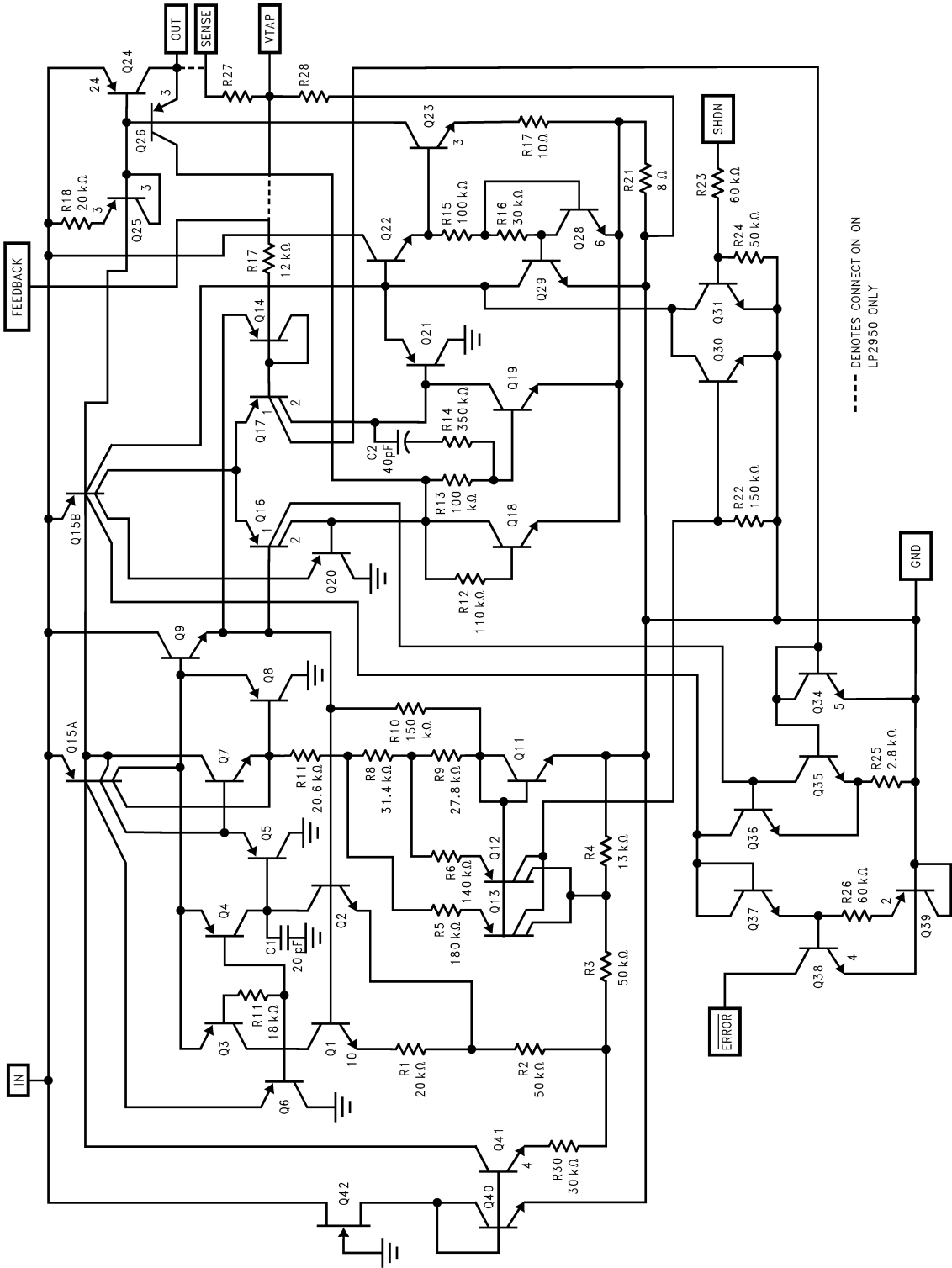


****Sets disconnect Hysteresis**

854618

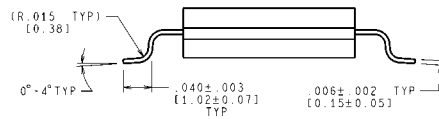
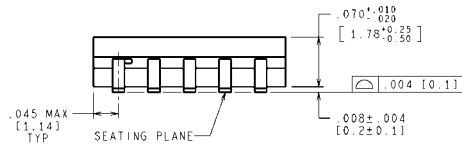
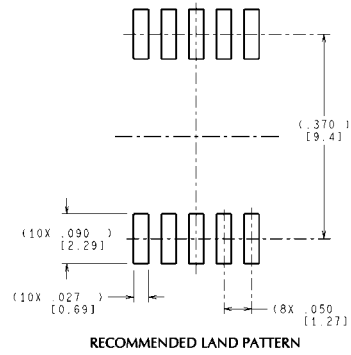
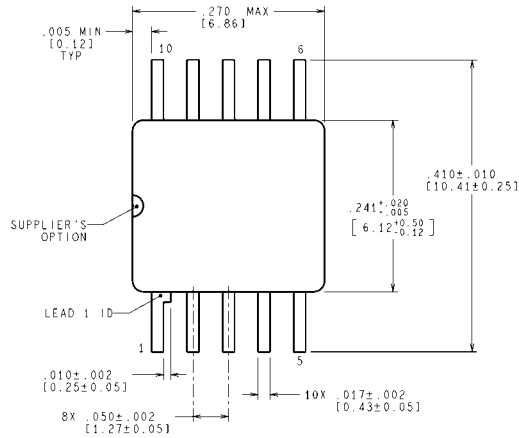
www.national.com

Schematic Diagram



----- DENOTES CONNECTION ON
LP2950 ONLY

Physical Dimensions inches (millimeters) unless otherwise noted

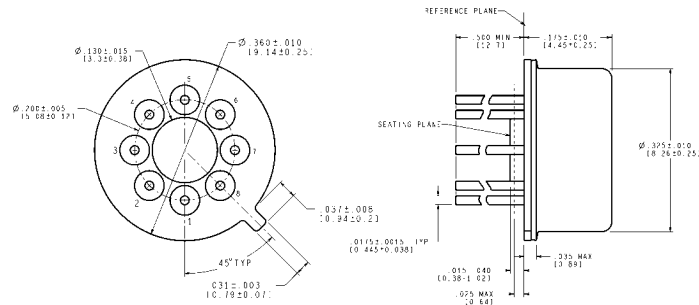


MIL-PRF-38535
CONFIGURATION CONTROL

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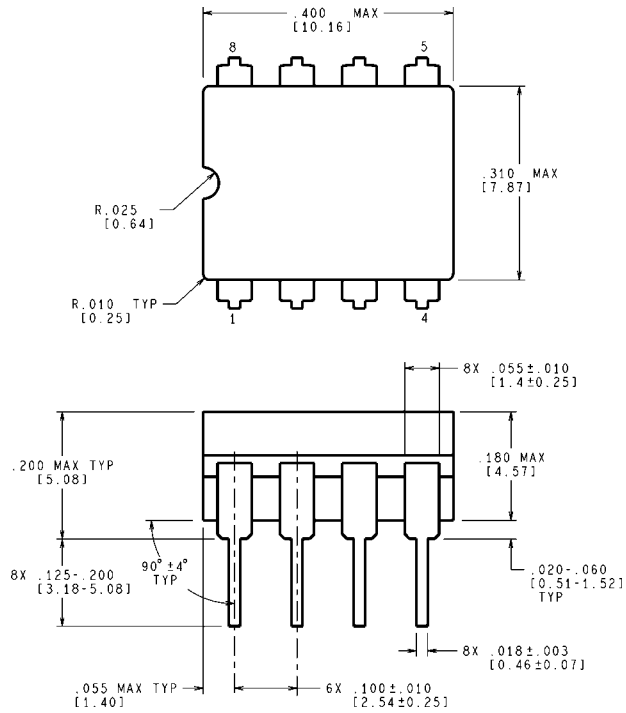
WG10A (Rev F)

Order Number LP2951WG/883
NS Package Number WG10A



Metal Can Package (H)
NS Package Number H08C

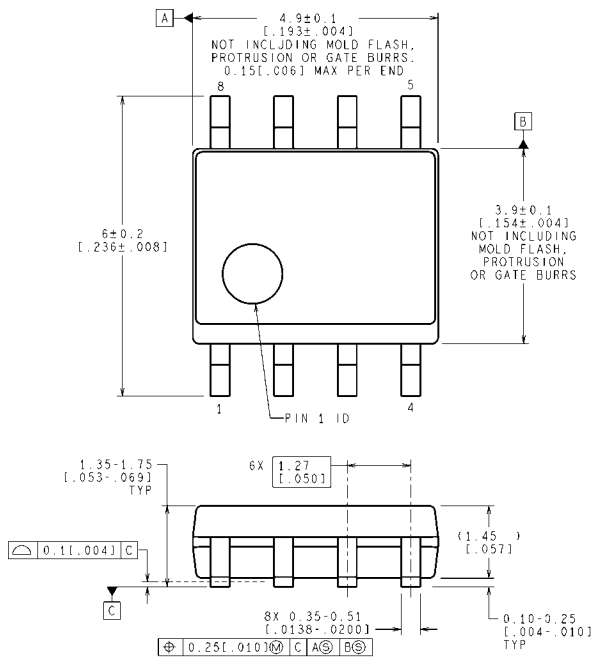
H08C (Rev F)



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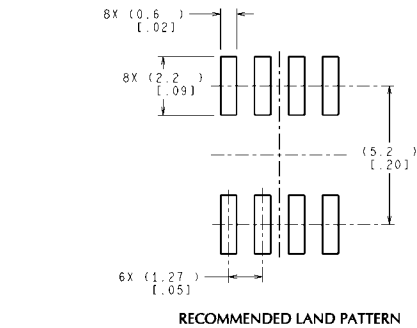
J08A (Rev M)

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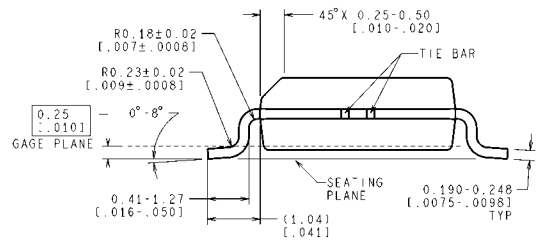


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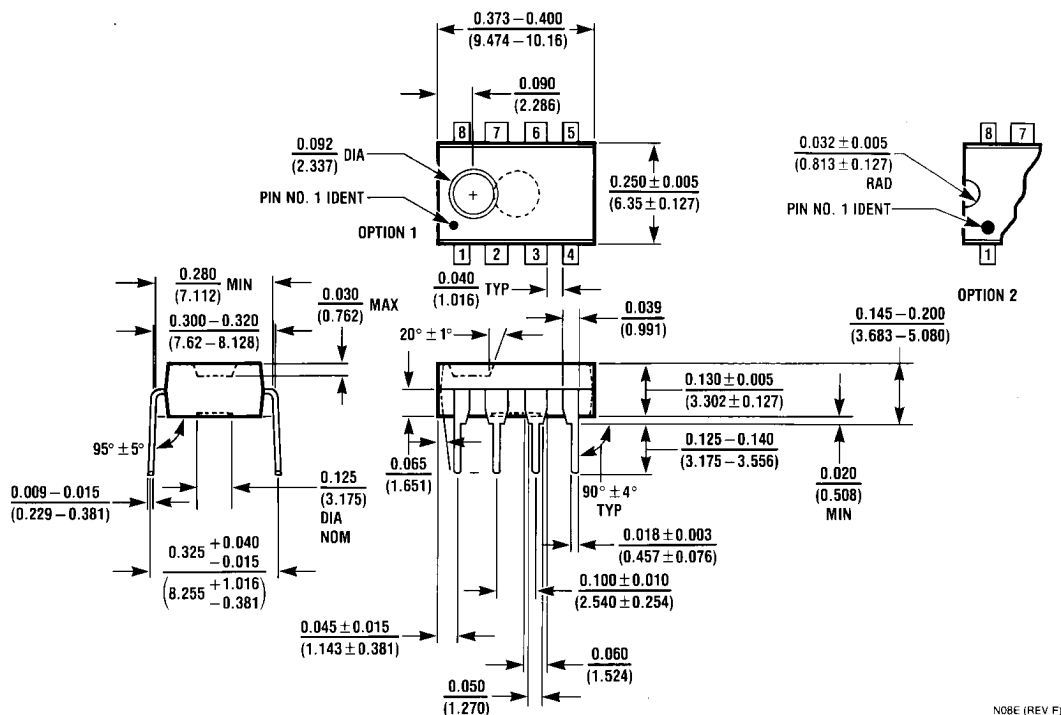
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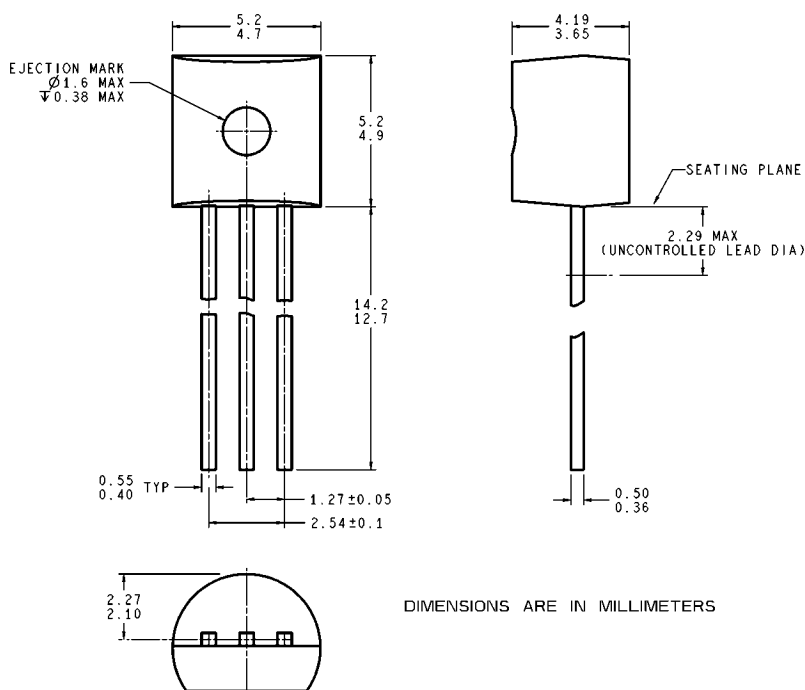
RECOMMENDED LAND PATTERN



M08A (Rev M)



Molded Dual-In-Line Package (N)
NS Package Number N08E



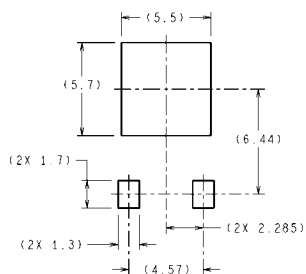
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Z03A (Rev G)

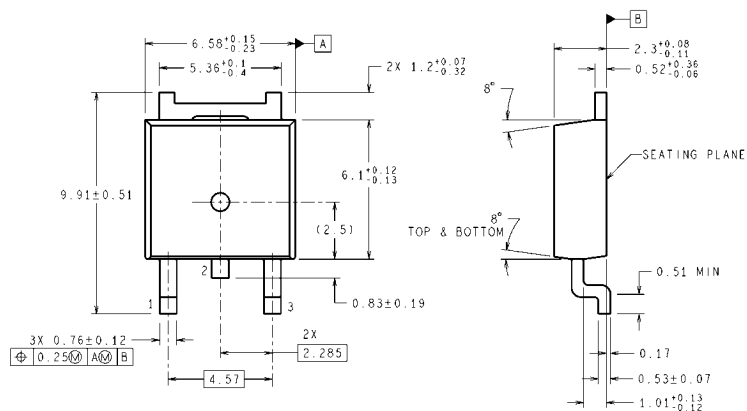
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VALUES IN [] ARE MILLIMETERS

Surface Mount Package (MM)
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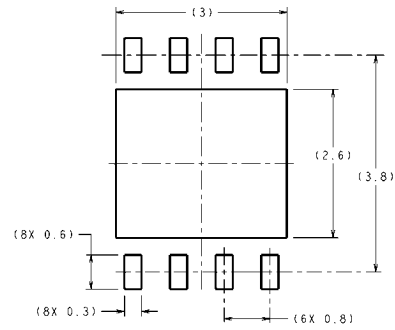
MUA08A (Rev F)



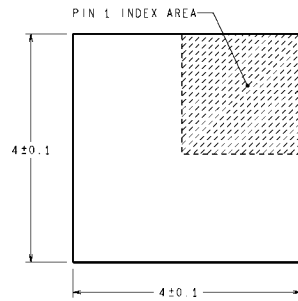
LAND PATTERN RECOMMENDATION



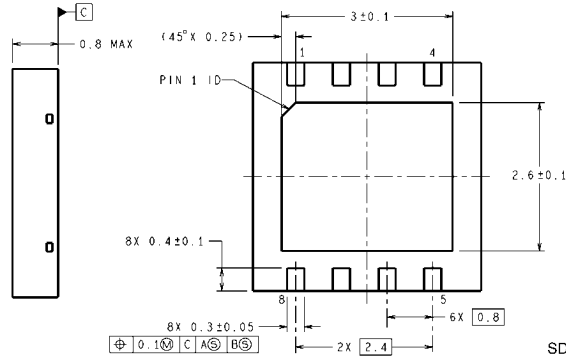
TD03B (Rev E)



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



SDC08A (Rev A)

LLP Package
NS Package Number SDC08A

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