

Video analog input interface**TDA8709A****FEATURES**

- 8-bit resolution
- Sampling rate up to 32 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low-level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs.

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing.
- Colour difference signals (U, V)
- R, G, B signals
- Chrominance signal (C).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CCA}	analog supply voltage	4.5	5.0	5.5	V
V _{CCD}	digital supply voltage	4.5	5.0	5.5	V
V _{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I _{CCA}	analog supply current	—	40	47	mA
I _{CCD}	digital supply current	—	24	30	mA
I _{CCO}	TTL output supply current	—	12	16	mA
ILE	DC integral linearity error	—	—	±1	LSB
DLE	DC differential linearity error	—	—	±0.5	LSB
f _{clk(max)}	maximum clock frequency	30	32	—	MHz
B	maximum -3 dB bandwidth (preamplifier)	12	18	—	MHz
P _{tot}	total power dissipation	—	380	512	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709A	28	DIP	plastic	SOT117-1
TDA8709AT	28	SO28L	plastic	SOT136-1

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BLOCK DIAGRAM

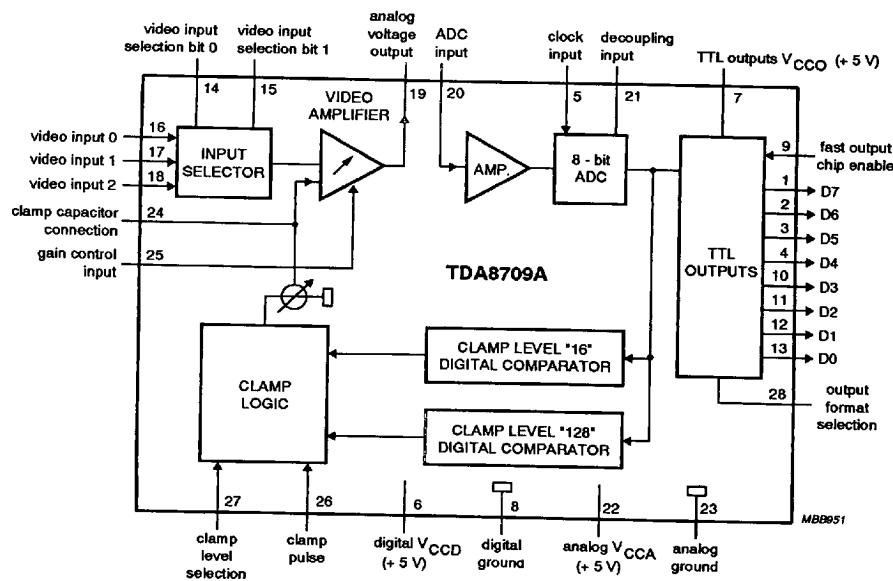


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V _{CCD}	6	digital supply voltage (+5 V)
V _{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video Input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V _{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamping pulse
CLS	27	clamping level selection input
OFS	28	output format selection

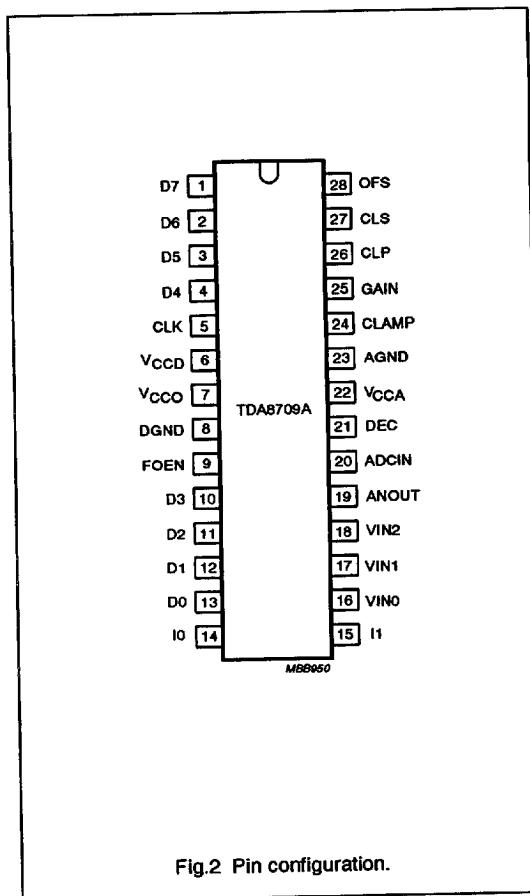


Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

TDA8709A is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for R, G, B signals) and digital 128 (for

chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamping level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	-0.3	+7.0	V
V_{CCD}	digital supply voltage	-0.3	+7.0	V
V_{CCO}	TTL output supply voltage	-0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	-0.5	+0.5	V
	supply voltage difference between V_{CCO} and V_{CCD}	-0.5	+0.5	V
	supply voltage difference between V_{CCA} and V_{CCO}	-1.0	+1.0	V
V_I	input voltage	-0.3	+7.0	V
	output current	-	+10	mA
T_{STG}	storage temperature	-55	+150	°C
T_{AMB}	operating ambient temperature	0	+70	°C
T_J	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ J-A}$	thermal resistance from junction to ambient in free air SOT117-1 SOT136-1	55 70	K/W K/W

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CHARACTERISTICS

$V_{CCA} = V_{22}$ to $V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6$ to $V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7$ to $V_9 = 4.2$ to 5.5 V; AGND and DGND shorted together; V_{CCA} to $V_{CCD} = -0.5$ to $+0.5$ V; V_{CCO} to $V_{CCD} = -0.5$ to $+0.5$ V; V_{CCA} to $V_{CCO} = -0.5$ to $+0.5$ V; $T_{amb} = 0$ to $+70$ °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		-	40	47	mA
I_{CCD}	digital supply current		-	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.7)	-	12	16	mA
Preamplifier Inputs						
VIN0 TO VIN2 INPUTS						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	note 1	0.6	-	1.5	V
$ Z_i $	input impedance	$f_i = 6$ MHz	10	20	-	kΩ
C_i	input capacitance	$f_i = 6$ MHz	-	1	-	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	V_{CCD}	V
I_{IL}	LOW level input current	$V_i = 0.4$ V	-400	-	-	μA
I_{IH}	HIGH level input current	$V_i = 2.7$ V	-	-	20	μA
CLS, OFS AND CLP TTL INPUTS (SEE Fig.5)						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	V_{CCD}	V
I_{IL}	LOW level input current	$V_i = 0.4$ V	-400	-	-	μA
I_{IH}	HIGH level input current	$V_i = 2.7$ V	-	-	20	μA
t_{CLP}	clamp pulse width		2	-	-	μs
GAIN INPUT (PIN 25)						
$V_{25(min)}$	input voltage for minimum gain	see Fig.9	-	1.8	-	V
$V_{25(max)}$	input voltage for maximum gain	see Fig.9	-	3.8	-	V
I_g	input current		-	1.0	-	μA
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		-	3.5	-	V
I_{24}	clamp output current			see Table 2		

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	$V_{OF} = 1.33 \text{ V (p-p)}$; $V_{25} = 3.0 \text{ V}$	-	1.33	-	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	-	mA
$I_{O(p-p)}$	output current driven by the load	$V_{ANOUT} = 1.33 \text{ V (p-p)}$; note 2	-	-	1.0	mA
V_{19}	DC output voltage for black level	CLS = logic 1	-	$V_{CCA} - 2.02$	-	V
V_{19}	DC output voltage for black level	CLS = logic 0	-	$V_{CCA} - 2.6$	-	V
Z_{19}	output impedance		-	20	-	Ω
Preamplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	$V_{CCA} = 4.75 \text{ to } 5.25 \text{ V}$; note 3	-	-50	-45	dB
G_{diff}	differential gain	$V_{VIN} = 1.33 \text{ V (p-p)}$; $V_{25} = 3.0 \text{ V}$	-	2	-	%
Φ_{diff}	differential phase	$V_{VIN} = 1.33 \text{ V (p-p)}$; $V_{25} = 3.0 \text{ V}$	-	0.8	-	deg
B	-3 dB bandwidth		12	-	-	MHz
S/N	signal-to-noise ratio	note 4	60	-	-	dB
SVRR1	supply voltage ripple rejection	note 5	-	45	-	dB
ΔG	gain range	see Fig.9	-4.5	-	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.9	-	-	5	%
Analog-to-digital converter Inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	V_{CCD}	V
I_{IL}	LOW level input current	$V_{clk} = 0.4 \text{ V}$	-400	-	-	μA
I_{IH}	HIGH level input current	$V_{clk} = 2.7 \text{ V}$	-	-	100	μA
$ Z_i $	input impedance	$f_{clk} = 10 \text{ MHz}$	-	4	-	$\text{k}\Omega$
C_i	input capacitance	$f_{clk} = 10 \text{ MHz}$	-	4.5	-	pF
FOEN INPUT (SEE TABLE 3)						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	V_{CCD}	V
I_{IL}	LOW level input current	$V_g = 0.4 \text{ V}$	-400	-	-	μA
I_{IH}	HIGH level input current	$V_g = 2.7 \text{ V}$	-	-	20	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 4)						
V_{20}	input voltage	digital output = 00	-	$V_{CCA} - 2.52$	-	V
V_{20}	input voltage	digital output = 255	-	$V_{CCA} - 1.52$	-	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		-	1.0	-	V
I_{20}	input current		-	1.0	10	μA
$ Z_i $	input impedance	$f_i = 6 \text{ MHz}$	-	50	-	$M\Omega$
C_i	input capacitance	$f_i = 6 \text{ MHz}$	-	1	-	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	$I_{OL} = 2 \text{ mA}$	0	-	0.6	V
V_{OH}	HIGH level output voltage	$I_{OL} = -0.4 \text{ mA}$	2.4	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	$0.4 \text{ V} < V_O < V_{CCD}$	-20	-	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.5; note 6	30	32	-	MHz
Analog signal processing ($f_{clk} = 32 \text{ MHz}$; see Fig.7)						
G_{diff}	differential gain	$V_{20} = 1.0 \text{ V (p-p)}$; see Fig.6; note 7	-	2	-	%
φ_{diff}	differential phase	see Fig.6; note 7	-	2	-	deg
f_1	fundamental harmonics (full-scale)	$f_i = 4.43 \text{ MHz}$; note 7	-	-	0	dB
f_{all}	harmonics (full-scale); all components	$f_i = 4.43 \text{ MHz}$; note 7	-	-55	-	dB
SVRR2	supply voltage ripple rejection	note 8	-	1	5	%/V
Transfer function						
ILE	DC integral linearity error		-	-	± 1	LSB
DLE	DC differential linearity error		-	-	± 0.5	LSB
ILE	AC integral linearity error	note 9	-	-	± 2	LSB
Timing ($f_{clk} = 32 \text{ MHz}$; see Figs 5, 6 and 7)						
DIGITAL OUTPUTS ($C_L = 15 \text{ pF}$; $I_{OL} = 2 \text{ mA}$; $R_L = 2 \text{ k}\Omega$)						
t_{ds}	sampling delay time		-	2	-	ns
t_h	output hold time		-	8	-	ns
t_d	output delay time		-	16	20	ns
t_{dEZ}	3-state delay time; output enable		-	16	25	ns
t_{dDZ}	3-state delay time; output disable		-	12	25	ns

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Notes to the "Characteristics"

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)} = 1.33$ V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
 - a) AC impedance ≥ 1 k Ω and the DC impedance > 2.7 k Ω .
 - b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Input signals with the same amplitude. Gain is adjusted to obtain $ANOUT = 1.33$ V (p-p).
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

$$\frac{S}{N} = 20 \log \frac{V_{ANOUT}(p-p)}{V_{ANOUT}(\text{RMS noise})} \text{ at } B = 5 \text{ MHz.}$$

5. The voltage ratio is expressed as:
$$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G} \text{ for } V_i = 1 \text{ V (p-p), gain at } 100 \text{ kHz} = 1 \text{ and } 1 \text{ V supply variation.}$$
6. It is recommended that the rise and fall times of the clock are ≥ 2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:
$$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) + (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$
9. Full-scale sine wave ($f_i = 4.4$ MHz; $f_{clk} = 27$ MHz).

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Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN1

Table 3 FOEN input coding.

FOEN	D0 TO D7
0	active, two's complement
1	high impedance

Table 2 CLAMP output current.

CLS	CLP	DIGITAL OUTPUT	I _{CLAMP}
1	1	output < 128	+50 µA
		output > 128	-50 µA
X ⁽¹⁾	0	X	0 µA
0	1	output < 16	+50 µA
		16 < output	-50 µA

Note

1. X = don't care.

Table 4 Output coding and input voltage (typical values).

STEP	V _{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	-	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V _{CCA} - 2.52 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	-	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	-
.	-
254	-	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V _{CCA} - 1.52 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	-	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

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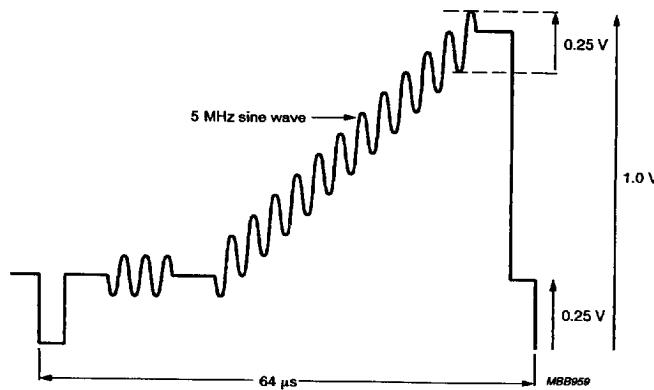


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

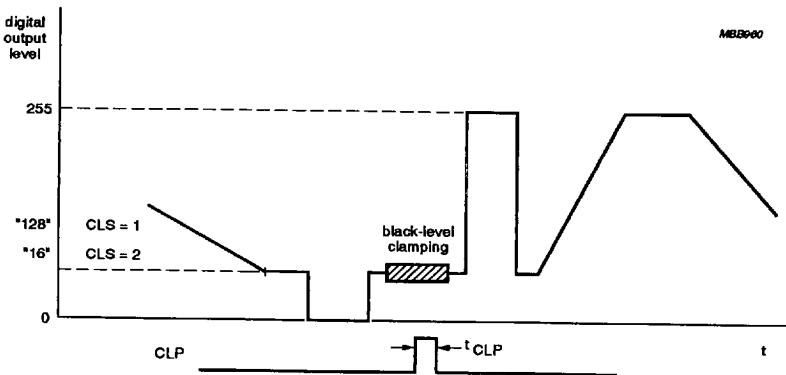


Fig.4 Control mode selection.

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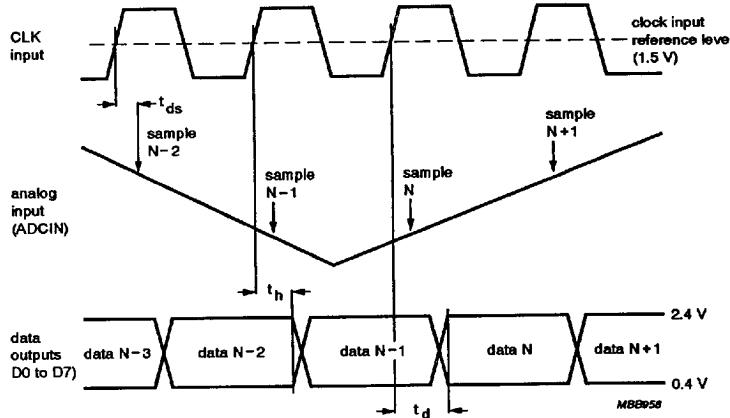


Fig.5 Timing diagram.

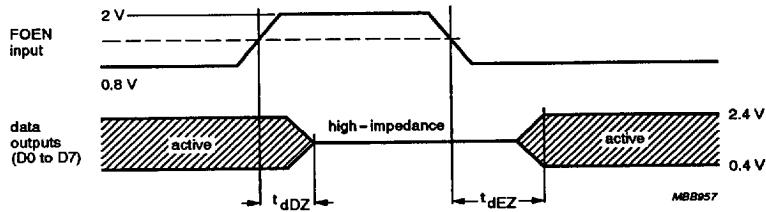


Fig.6 Output format timing diagram.

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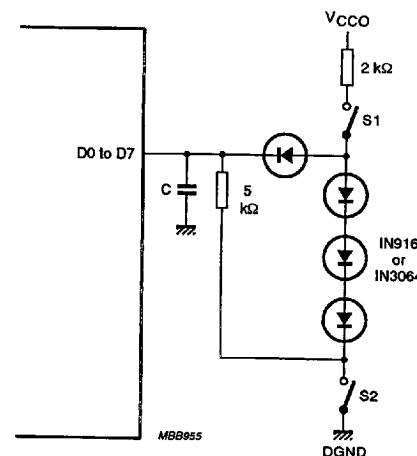
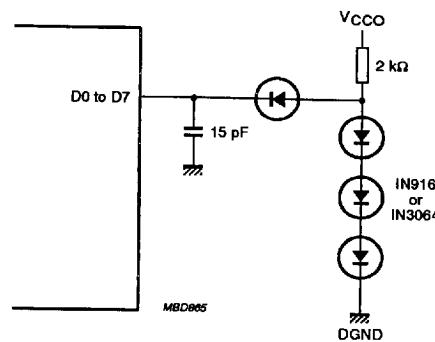


Fig.7 Load circuit for timing measurement; data outputs (FOEN = LOW).

Fig.8 Load circuit for timing measurement; 3-state outputs (FOEN: $f_i = 1$ MHz; $V_{FOEN} = 3$ V).

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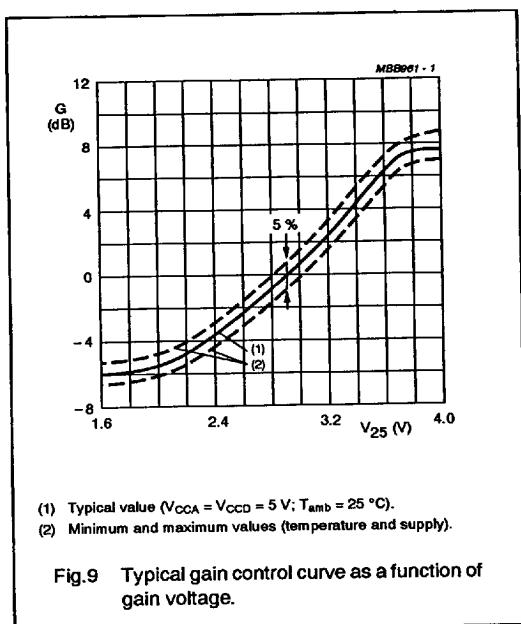


Fig.9 Typical gain control curve as a function of gain voltage.

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INTERNAL PIN CIRCUITRY

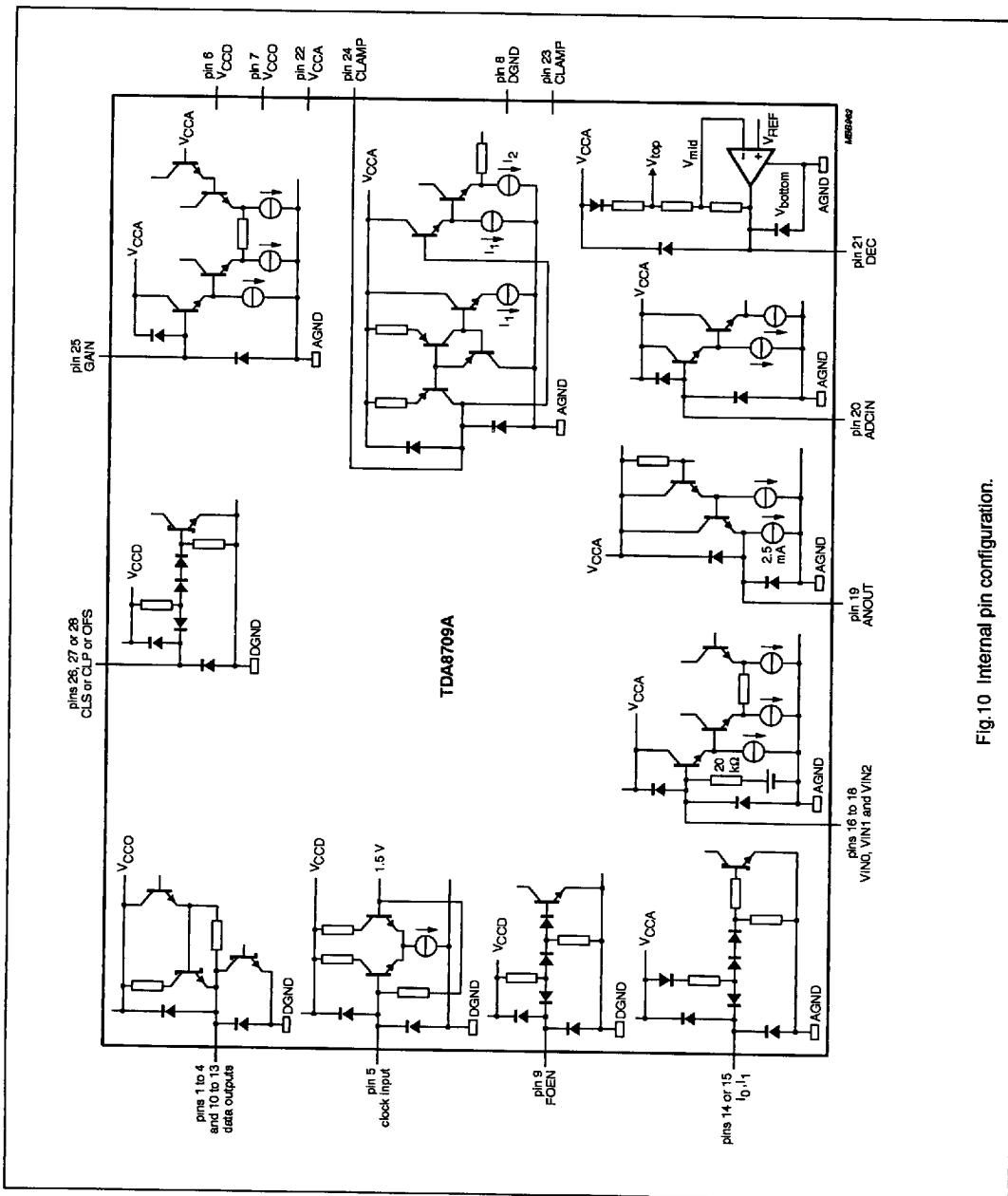


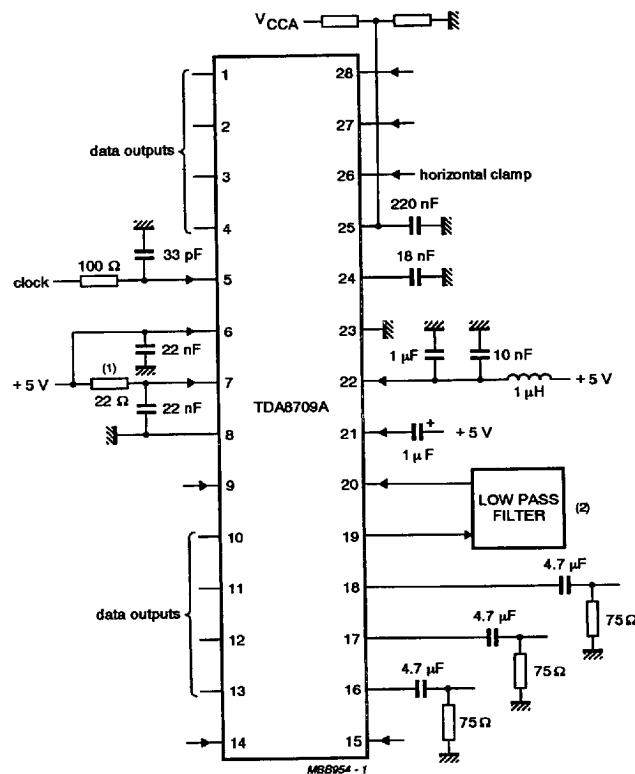
Fig.10 Internal pin configuration.

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APPLICATION INFORMATION

Additional information can be found in the laboratory report of TDA8708A "FBL/AN9308".

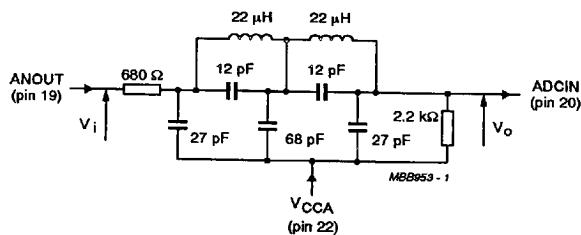


- (1) It is recommended to decouple V_{CCO} through a $22\ \Omega$ resistor especially when the output data of TDA8709A interfaces with a capacitive CMOS load device.
- (2) See Figs 12, 14, 16 and 18 for examples of the low-pass filters.

Fig.11 Application diagram.

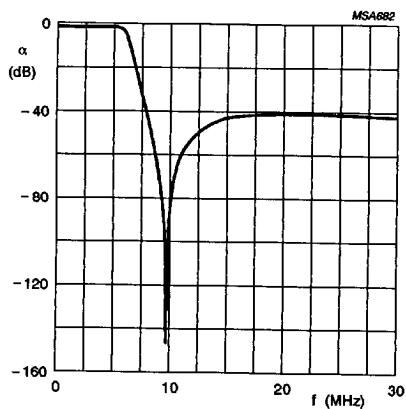
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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least $680\ \Omega$ and $2.2\ k\Omega$ must in any event be applied.

Fig.12 Example of a low-pass filter for RGB and C signals.



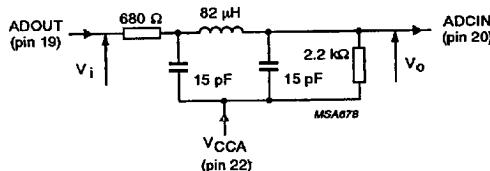
Characteristics of Fig.13

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- $f = 6.5$ MHz at -3 dB
- $f_{\text{notch}} = 9.65$ MHz.

Fig.13 Frequency response for filter shown in Fig.12.

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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680Ω and $2.2 \text{ k}\Omega$ must in any event be applied.

Fig.14 Example of an economical low-pass filter for RGB and C signals.

Characteristics of Fig.15

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4 \text{ dB}$
- $f = 6.5 \text{ MHz}$ at -3 dB .

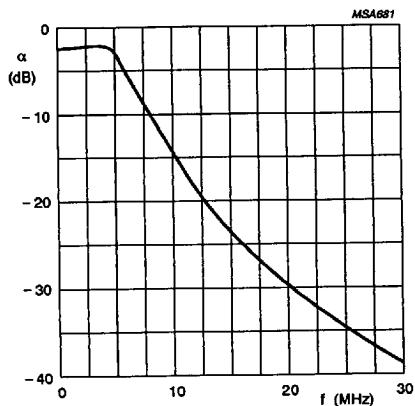
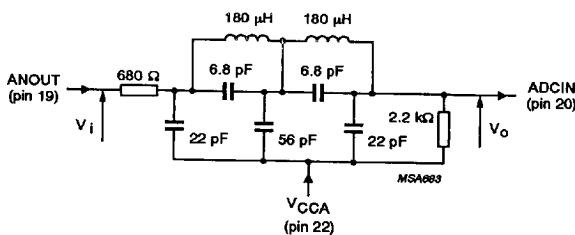


Fig.15 Frequency response for filter shown in Fig.14.

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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least $680\ \Omega$ and $2.2\ k\Omega$ must in any event be applied.

Fig.16 Example of a low-pass filter for U and V signals.

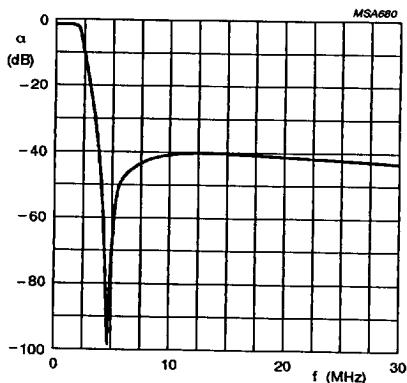


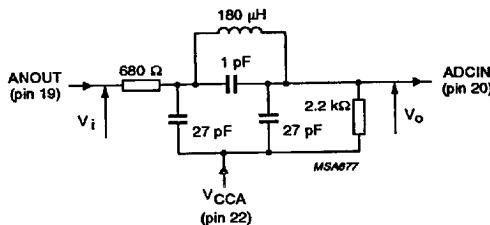
Fig.17 Frequency response for filter shown in Fig.16.

Characteristics of Fig.17

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- $f = 2.3$ MHz at -3 dB
- $f_{\text{notch}} = 4.5$ MHz.

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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least $680\ \Omega$ and $2.2\ k\Omega$ must in any event be applied.

Fig.18 Example of an economical low-pass filter for U and V signals.

Characteristics of Fig.19

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.3\ dB$
- $f = 2.8\ MHz$ at $-3\ dB$
- $f_{notch} = 11.9\ MHz$.

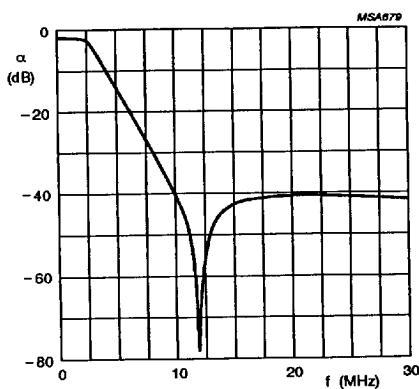


Fig.19 Frequency response for filter shown in Fig.18.