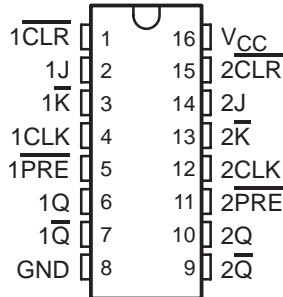


SN54HC109, SN74HC109 DUAL J-K̄ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

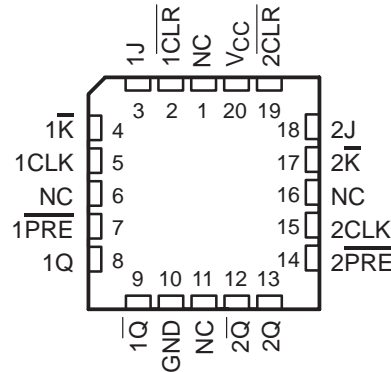
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- Wide Operating Voltage Range of 2 V to 6 V
- Low Input Current of 1 μ A Max
- High-Current Outputs Drive Up To 10 LSTTL Loads
- Low Power Consumption, 40- μ A Max I_{CC}
- Typical $t_{pd} = 12$ ns
- ± 4 -mA Output Drive at 5 V

SN54HC109 . . . J OR W PACKAGE
SN74HC109 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54HC109 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain two independent J-K̄ positive-edge-triggered flip-flops. A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the J and \overline{K} inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the J and \overline{K} inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding \overline{K} and tying J high. They also can perform as D-type flip-flops if J and \overline{K} are tied together.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC109N | SN74HC109N |
| | SOIC – D | Tube of 40 | SN74HC109D | HC109 |
| | | Reel of 2500 | SN74HC109DR | |
| | | Reel of 250 | SN74HC109DT | |
| SOP – NS | Reel of 2000 | SN74HC109NSR | HC109 | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC109J | SNJ54HC109J |
| | CFP – W | Tube of 150 | SNJ54HC109W | SNJ54HC109W |
| | LCCC – FK | Tube of 55 | SNJ54HC109FK | SNJ54HC109FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC109, SN74HC109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

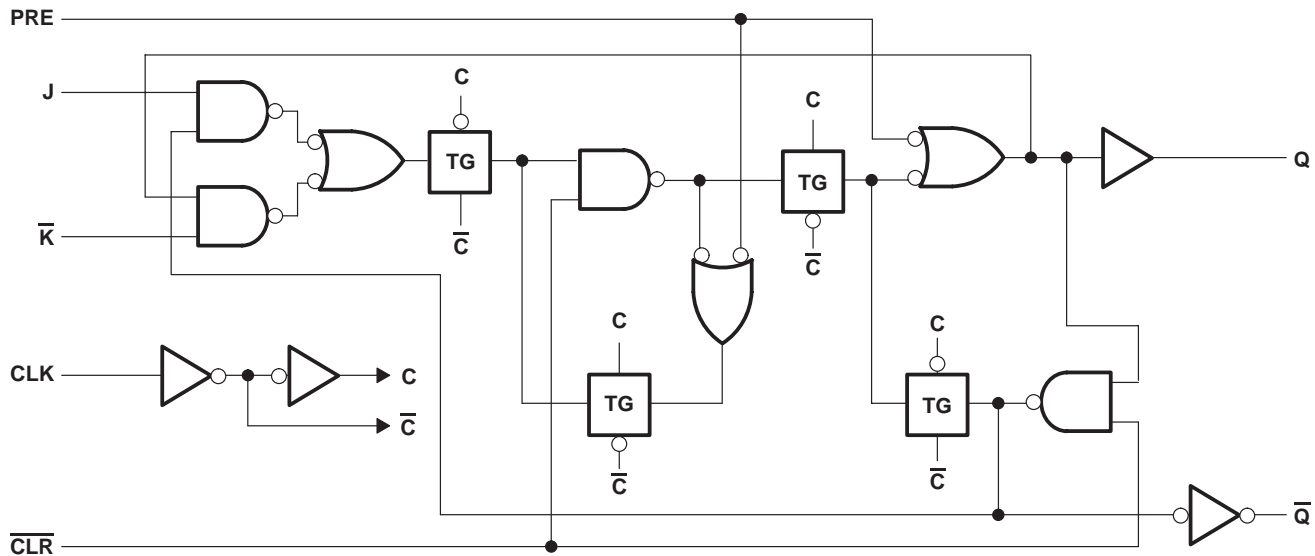
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FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | |
|-------------------------|-------------------------|-----|---|-----------------------|---------|------------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | J | $\overline{\text{K}}$ | Q | $\overline{\text{Q}}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | Toggle | |
| H | H | ↑ | L | H | Q0 | $\overline{\text{Q}}0$ |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | Q0 | $\overline{\text{Q}}0$ |

† This configuration is nonstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

logic diagram, each flip-flop (positive logic)



SN54HC109, SN74HC109

DUAL J-K̄ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±35 mA |
| Continuous current through V_{CC} or GND | ±70 mA |
| Package thermal impedance, θ_{JA} (see Note 1): D package | 73°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK, J, or W packages | 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or NS packages | 260°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

| | | SN54HC109 | | | SN74HC109 | | | UNIT | |
|---------------------|---------------------------------|------------------|-----|----------|------------------|------------------|----------|------|----|
| | | MIN | NOM | MAX | MIN | NOM | MAX | | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V | |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | | 1.5 | $V_{CC} = 2$ V | | 1.5 | V | |
| | | $V_{CC} = 4.5$ V | | 3.15 | $V_{CC} = 4.5$ V | | 3.15 | | |
| | | $V_{CC} = 6$ V | | 4.2 | $V_{CC} = 6$ V | | 4.2 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | | 0.3 | $V_{CC} = 2$ V | | 0.5 | V |
| | | $V_{CC} = 4.5$ V | | | 0.9 | $V_{CC} = 4.5$ V | | 1.35 | |
| | | $V_{CC} = 6$ V | | | 1.2 | $V_{CC} = 6$ V | | 1.8 | |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V | |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V | |
| $\Delta t/\Delta v$ | Input transition rise/fall time | $V_{CC} = 2$ V | | | 1000 | $V_{CC} = 2$ V | | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | | 500 | $V_{CC} = 4.5$ V | | 500 | |
| | | $V_{CC} = 6$ V | | | 400 | $V_{CC} = 6$ V | | 400 | |
| T_A | Operating free-air temperature | –55 | | 125 | –40 | | 85 | °C | |

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54HC109, SN74HC109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HC109 | | SN74HC109 | | UNIT |
|-----------------|---|--------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | V | |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | | 0.1 |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | | 0.1 |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | | 0.33 |
| | | | 6 V | | 0.15 | 0.26 | | 0.4 | | | 0.33 |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | 4 | | 80 | | 40 | μA |
| C _i | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC109 | | SN74HC109 | | UNIT |
|--------------------|------------------------|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | | 6 | | 4.2 | | 5 | MHz |
| | | 4.5 V | | 31 | | 21 | | 25 | |
| | | 6 V | | 36 | | 25 | | 29 | |
| t _w | Pulse duration | PRE or CLR low | 2 V | 100 | | 150 | | 125 | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | |
| | | | 6 V | 17 | | 25 | | 21 | |
| | CLK high or low | 2 V | 80 | | 120 | | 100 | | |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| t _{su} | Setup time before CLK↑ | Data (J, K) | 2 V | 100 | | 150 | | 125 | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | |
| | | | 6 V | 17 | | 25 | | 21 | |
| | PRE or CLR inactive | 2 V | 25 | | 40 | | 30 | | |
| | | 4.5 V | 5 | | 8 | | 6 | | |
| | | 6 V | 4 | | 7 | | 5 | | |
| t _h | Hold time | Data after CLK↑ | 2 V | 0 | | 0 | | 0 | ns |
| | | | 4.5 V | 0 | | 0 | | 0 | |
| | | | 6 V | 0 | | 0 | | 0 | |



SN54HC109, SN74HC109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HC109 | | SN74HC109 | | UNIT |
|------------------|--|---------------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | 2 V | 6 | 10 | | 4.2 | | 5 | ns | |
| | | | 4.5 V | 31 | 50 | | 21 | | 25 | | |
| | | | 6 V | 36 | 60 | | 25 | | 29 | | |
| t _{pd} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or \overline{Q} | 2 V | | 60 | 230 | | 345 | | 290 | ns |
| | | | 4.5 V | | 15 | 46 | | 69 | | 58 | |
| | | | 6 V | | 12 | 39 | | 59 | | 49 | |
| | CLK | Q or \overline{Q} | 2 V | | 50 | 175 | | 250 | | 220 | |
| | | | 4.5 V | | 15 | 35 | | 50 | | 44 | |
| | | | 6 V | | 12 | 30 | | 42 | | 37 | |
| t _t | | Q or \overline{Q} | 2 V | | 28 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

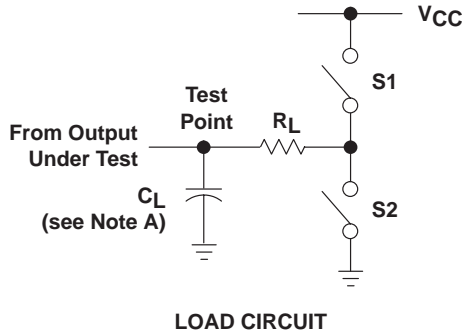
operating characteristics, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------|-----|------|
| C _{pd} Power dissipation capacitance per buffer/driver | No load | 35 | pF |

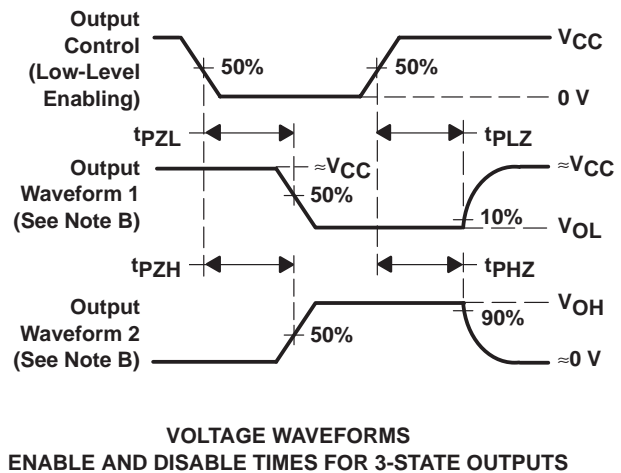
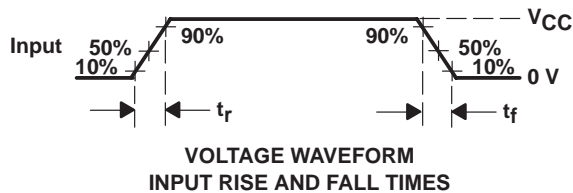
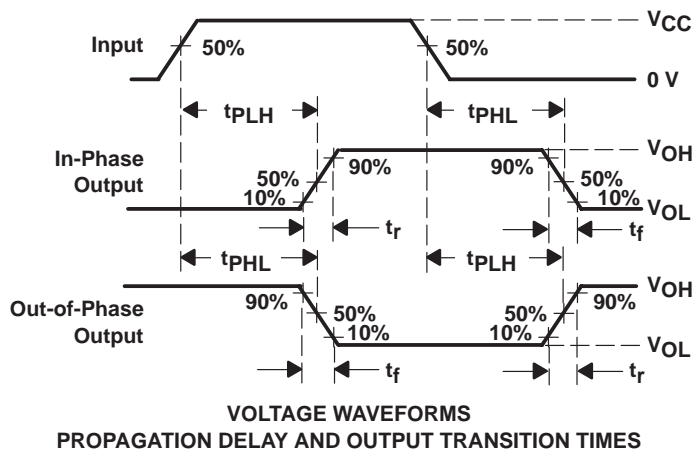
SN54HC109, SN74HC109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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PARAMETER MEASUREMENT INFORMATION



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | -- | 50 pF or 150 pF | Open | Open |



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-8415001VEA | ACTIVE | CDIP | J | 16 | 25 | TBD | A42 | N / A for Pkg Type | |
| 5962-8415001VFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| 84150012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Call TI | |
| 8415001EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Call TI | |
| 8415001FA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Call TI | |
| JM38510/65304B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| JM38510/65304BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/65304B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| M38510/65304BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54HC109J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN74HC109D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109DT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109DTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109DTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74HC109NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74HC109NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| SN74HC109NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC109NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SNJ54HC109FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54HC109J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54HC109W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54HC109, SN54HC109-SP, SN74HC109 :

- Catalog: [SN74HC109](#), [SN54HC109](#)

- Military: [SN54HC109](#)
- Space: [SN54HC109-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC109DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC109NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

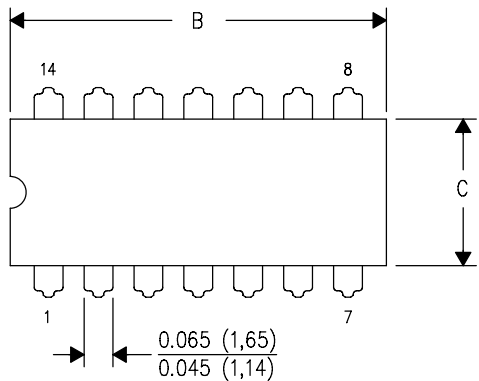


*All dimensions are nominal

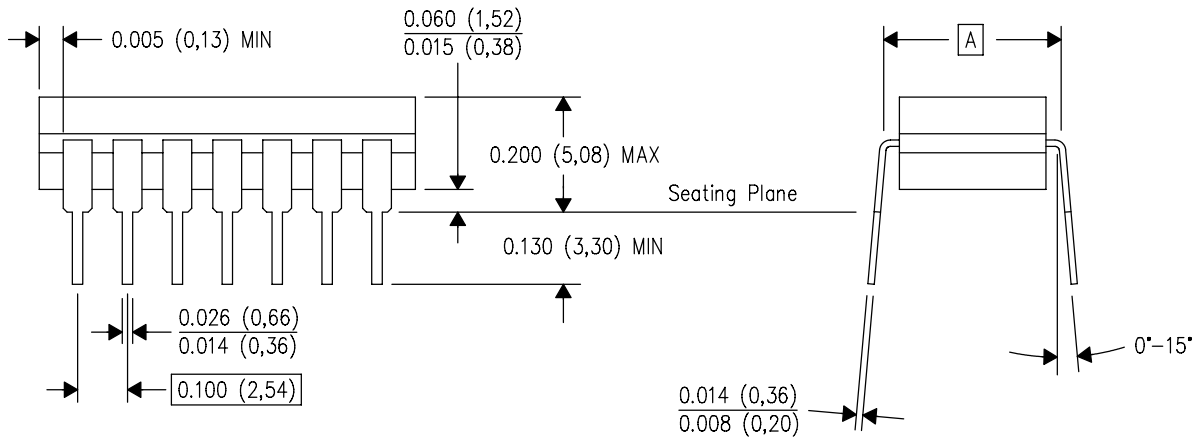
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC109DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC109NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



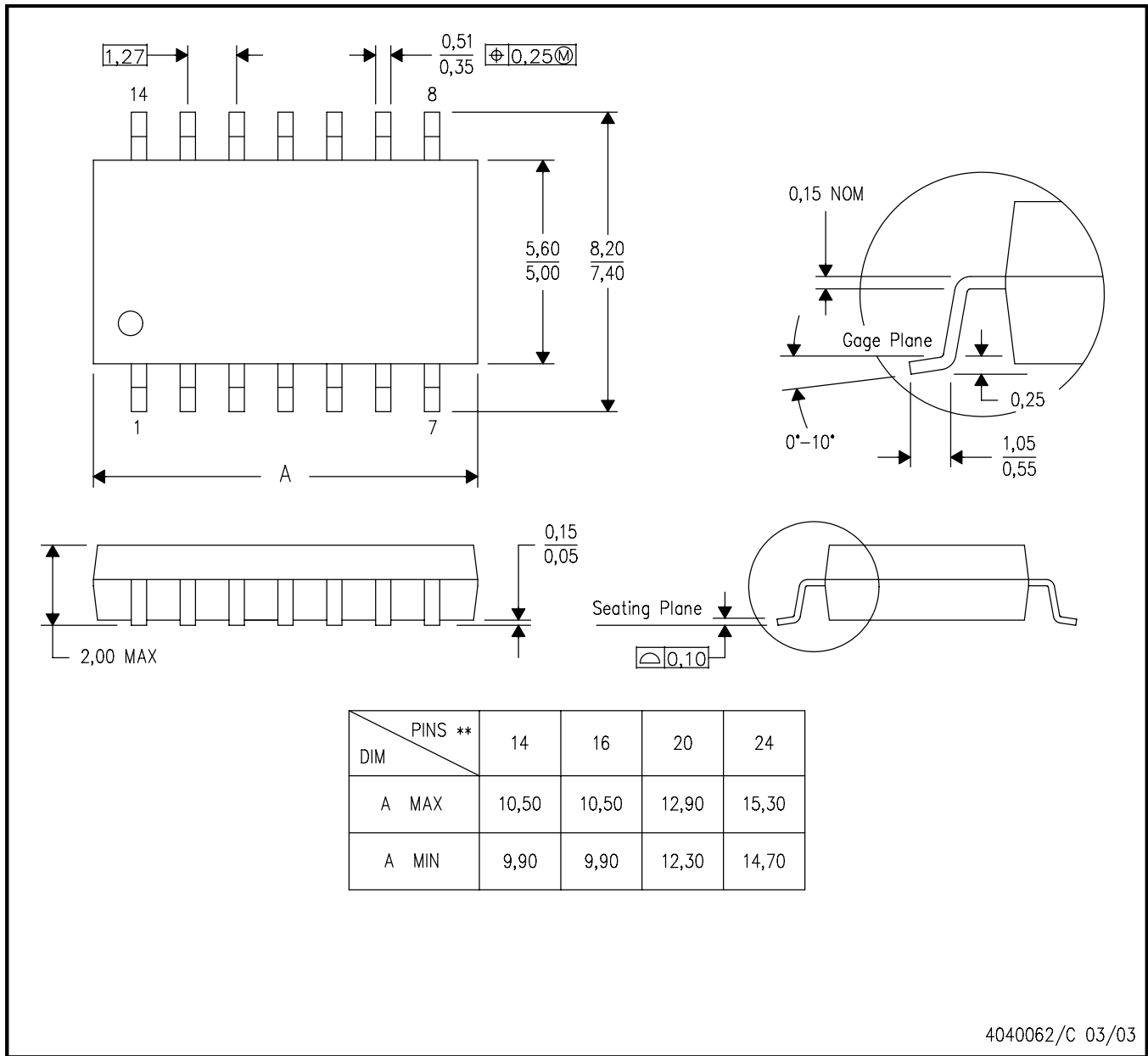
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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