

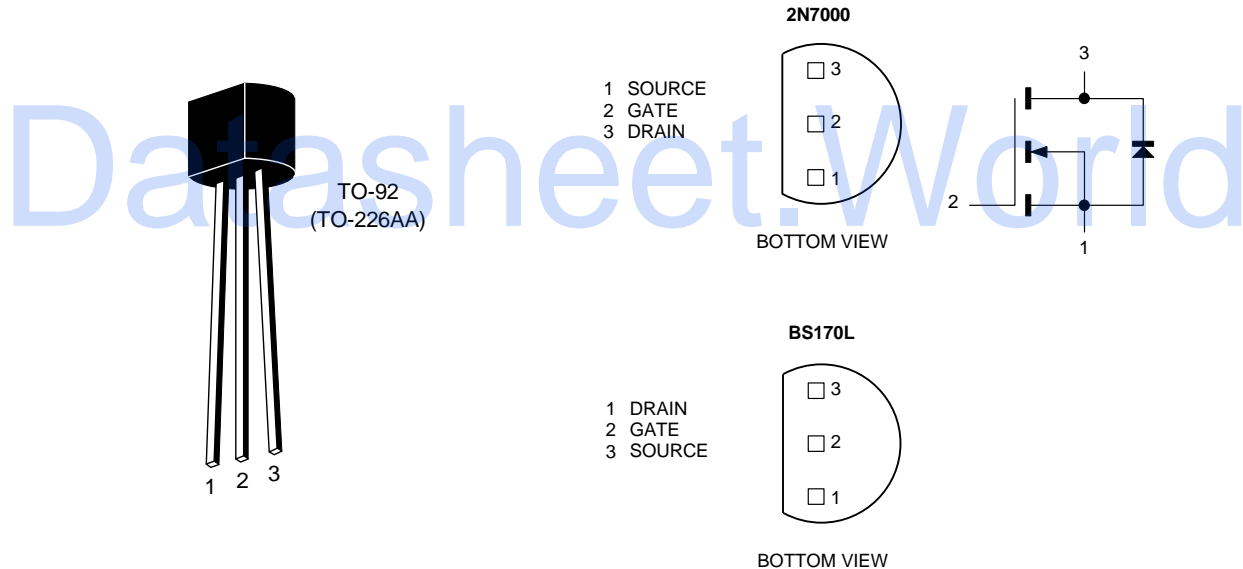
DESCRIPTION

The 2N7000 utilizes Calogic's vertical DMOS technology. The device is well suited for switching applications where B_V of 60V and low on resistance (under 5 ohms) are required. The 2N7000 is housed in a plastic TO-92 package.

ORDERING INFORMATION

Part	Package	Temperature Range
2N7000	Plastic TO-92	-55°C to +150°C
BS170L	Plastic TO-92	-55°C to +150°C
X2N7000	Sorted Chips in Carriers	-55°C to +150°C

PIN CONFIGURATION



CD5

PRODUCT SUMMARY

P/N	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
2N7000	60	5	0.2
BS170	60	5	0.5

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETERS	LIMITS	UNITS	TEST CONDITIONS
V _{DS}	Drain-Source Voltage	60	V	
V _{GS}	Gate-Source Voltage	±40		
I _D	Continuous Drain Current	0.2	A	T _A = 25°C
		0.13		T _A = 100°C
I _{DM}	Pulsed Drain Current ¹	0.5		
P _D	Power Dissipation ¹	0.4	W	T _A = 25°C
		0.16		T _A = 100°C
T _J	Operating Junction Temperature Range	-55 to 150	°C	
T _{stg}	Storage Temperature Range	-55 to 150		
T _L	Lead Temperature (1/16" from case for 10 sec.)	300		

THERMAL RESISTANCE RATINGS

SYMBOL	THERMAL RESISTANCE	LIMITS	UNITS
R _{thJA}	Junction-to-Ambient	312.5	K/W

NOTE: 1. Pulse width limited by maximum junction temperature.

SPECIFICATIONS¹

SYMBOL	PARAMETER	MIN	TYP ²	MAX	UNIT	TEST CONDITIONS
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	60	70		V	I _D = 10μA, V _{GS} = 0V
V _{GS(th)}	Gate-Threshold Voltage	0.8	1.9	3		V _{DS} = V _{GS} , I _D = 1mA
I _{GSS}	Gate-Body Leakage			±10	nA	V _{GS} = ±15V, V _{DS} = 0V
I _{DSS}	Zero Gate Voltage Drain Current			1	μA	V _{DS} = 48V, V _{GS} = 0V T _C = 125°C
		1000				
I _{D(ON)}	On-State Drain Current ³	75	210		mA	V _{DS} = 10V, V _{GS} = 4.5V
r _{DS(ON)}	Drain-Source On-Resistance ³		4.8	5.3	Ω	⁴ V _{GS} = 4.5V, I _D = 75mA
			2.5	5		V _{GS} = 10V, I _D = 0.5A
			4.4	9		T _C = 125°C
V _{DS(ON)}	Drain-Source On-Voltage ³		0.36	0.4	V	⁴ V _{GS} = 4.5V, I _D = 75mA
			1.25	2.5		V _{GS} = 10V, I _D = 0.5A
			2.2	4.5		T _C = 125°C ⁴
g _{FS}	Forward Transconductance ³	100	170		mS	V _{DS} = 10V, I _D = 0.2A
g _{OS}	Common Source Output Conductance ^{3,4}		500		μS	V _{DS} = 5V, I _D = 50mA
DYNAMIC						
C _{iss}	Input Capacitance		16	60	pF	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz
C _{oss}	Output Capacitance ⁴		11	25		
C _{rss}	Reverse Transfer Capacitance		2	5		
SWITCHING						
t _{ON}	Turn-On Time		7	10	nS	V _{DD} = 15V, R _L = 25Ω, I _D = 0.5A V _{GEN} = 10V, R _G = 25Ω (Switching time is essentially independent of operating temperature)
t _{OFF}	Turn-Off Time		7	10		

- NOTES: 1. T_A = 25°C unless otherwise specified.
 2. For design aid only, not subject to production testing.
 3. Pulse test; PW = ≤300μS, duty cycle ≤3%.
 4. This parameter not registered with JEDEC.