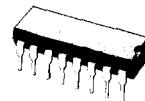


50 V - 1.5 A QUAD DARLINGTON SWITCHES

JPUT CURRENT TO 1.5 A EACH DARLING-
 N
 NIMUM BREAKDOWN 50 V
 ISTAINING VOLTAGE AT LEAST 35 V
 TEGRAL SUPPRESSION DIODES
 _LN2064B, ULN2066B, ULN2068B and
 N2070B)
 OLATED DARLINGTON PINOUT
 _LN2074B, ULN2076B)
 RSIONS COMPATIBLE WITH ALL POPU-
 R LOGIC FAMILIES

tible with popular 5 V logic families and the
 ULN2066B and ULN2076B are compatible with 6-
 15 V CMOS and PMOS. Types ULN2068B and
 ULN2070B include a predriver stage to reduce load-
 ing on the control logic.

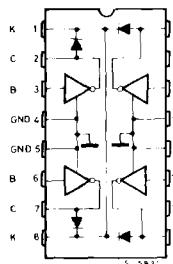


POWERDIP
 12 + 2 + 2

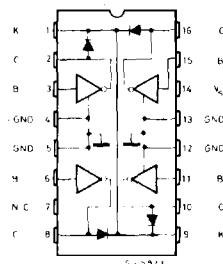
RIPTION

ned to interface logic to a wide variety of high
 it, high voltage loads, these devices each
 n four NPN darlington switches delivering up
 A with a specified minimum breakdown of 50
 a sustaining voltage of 35 V measured at 100
 he ULN2064B, ULN2066B, ULN2068B and
 070B contain integral suppression diodes for
 ve loads have common emitters. The
 074B and ULN2076B feature isolated darling-
 routs and are intended for applications such
 nitter follower configurations. Inputs of the
 064B, ULN2068B and ULN2074B are compa-

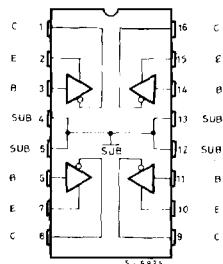
CONNECTIONS (top view) and ORDER CODES



ULN2064B
 ULN2068B



ULN2068B
 ULN2070B

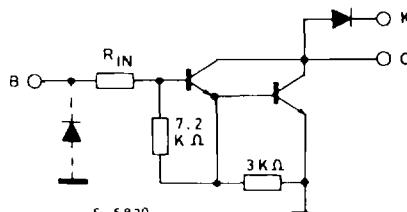


ULN2074B
 ULN2076B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	U
V_{CEX}	Output Voltage	50	
$V_{CE(sus)}$	Output Sustaining Voltage	35	
I_o	Output Current	1.75	
V_i	Input Voltage for ULN2066B/70B/74B/76B for ULN2064B/68B	30 15	
I_i	Input Current	25	I
V_s	Supply Voltage for ULN2068B for ULN2070B	10 20	
P_{tot}	Power Dissipation : at $T_{amb} = 90^{\circ}\text{C}$ at $T_{amb} = 70^{\circ}\text{C}$	4.3 1	
T_{amb}	Operating Ambient Temperature Range	- 20 to 85	
T_{stg}	Storage Temperature	- 55 to 150	

SCHEMATIC DIAGRAM



ULN2064B : $R_{IN} = 35 \Omega$
 ULN2066B : $R_{IN} = 3 \text{ k}\Omega$

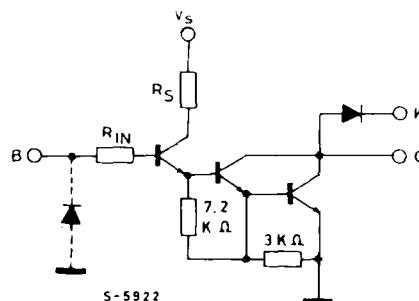
ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
(EX)	Output Leakage Current	for ULN2064B – ULN2066B $V_{CE} = 50 V$ $V_{CE} = 50 V$ $T_{amb} = 70^\circ C$		100 500	μA μA		1
(sus)	Collector-emitter Sustaining Voltage	for ULN2064B – ULN2066B $I_C = 100 mA$ $V = 0.4 V$	35			V	2
(sat)	Collector-emitter Saturation Voltage	$I_C = 500 mA$ $I_B = 625 \mu A$ $I_C = 750 mA$ $I_B = 935 \mu A$ $I_C = 1 A$ $I_B = 1.25 mA$ $I_C = 1.25 A$ $I_B = 2 mA$		1.1 1.2 1.3 1.4	V V V V		3
(in)	Input Current	for ULN2064B $V_i = 2.4 V$ for ULN2064B $V_i = 3.75 V$ for ULN2066B $V_i = 5 V$ for ULN2066B $V_i = 12 V$	1.4 3.3 0.6 1.7	4.3 9.6 1.8 5.2	mA mA mA mA		4
(in)	Input Voltage	for ULN2064B $V_{CE} = 2 V$ $I_C = 1 A$ $V_{CE} = 2 V$ $I_C = 1.5 A$ for ULN2066B $V_{CE} = 2 V$ $I_C = 1 A$ $V_{CE} = 2 V$ $I_C = 1.5 A$		2 2.5 6.5 10	V V V V		5
(tH)	Turn-on Delay Time	0.5 V_i to 0.5 V_o		1	ns		
(tL)	Turn-off Delay Time	0.5 V_i to 0.5 V_o		1.5	μs		
(I)	Clamp Diode Leakage Current	for ULN2064B – ULN2066B $V_R = 80 V$ $V_R = 80 V$ $T_{amb} = 70^\circ C$		50 100	μA μA		6
(F)	Clamp Diode Forward Voltage	$I_F = 1 A$ $I_F = 1.5 A$		1.75 2	V V		7

1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B and ULN2076B reference is ground for all other types.

2. Input current may be limited by maximum allowable input voltage.

CIRCUIT DIAGRAM

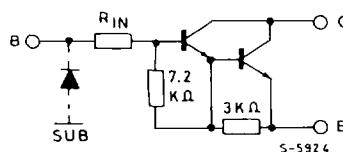


ULN2068B : $R_{IN} = 2.5 k\Omega$
ULN2070B : $R_{IN} = 11.6 k\Omega$

$R_S = 900 \Omega$
 $R_S = 3.4 k\Omega$

ELECTRICAL CHARACTERISTICS ($V_s = 5$ V for ULN2068B, $V_s = 12$ V for ULN2070B, $T_{amb} = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output Leakage Current	for ULN2068B – ULN2070B $V_{CE} = 50$ V $V_{CE} = 50$ V $T_{amb} = 70^\circ C$			100 500	μA μA
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for ULN2068B – ULN2070B $I_C = 100$ mA $V_i = 0.4$ V	35			V
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for ULN2068B $I_C = 500$ mA $V_i = 2.75$ V $I_C = 750$ mA $V_i = 2.75$ V $I_C = 1$ A $V_i = 2.75$ V $I_C = 1.25$ A $V_i = 2.75$ V for ULN2070B $I_B = 500$ mA $V_i = 5$ V $I_B = 750$ mA $V_i = 5$ V $I_B = 1$ A $V_i = 5$ V $I_B = 1.25$ A $V_i = 5$ V			1.1 1.2 1.3 1.4 1.1 1.2 1.3 1.4	V V V V V V V V
$I_{(on)}$	Input Current	for ULN2068B $V_i = 2.75$ V for ULN2068B $V_i = 3.75$ V for ULN2070B $V_i = 5$ V for ULN2070B $V_i = 12$ V			550 1000 400 1250	μA μA μA μA
$V_{i(on)}$	Input Voltage	$V_{CE} = 2$ V $I_C = 1.5$ A for ULN2068B for ULN2070B			2.75 5	V V
I_S	Supply Current	for ULN2068B $I_C = 500$ mA $V_i = 2.75$ V for ULN2070B $I_C = 500$ mA $V_i = 5$ V			6 4.5	mA mA
t_{PLH}	Turn-on Delay Time	0.5 V_o to 0.5 V_o			1	μs
t_{PHL}	Turn-off Delay Time	0.5 V_o to 0.5 V_o $I_C = 1.25$ A			1.5	μs
I_R	Clamp Diode Leakage Current	for ULN2068B – ULN2070B $V_R = 50$ V $V_R = 50$ V $T_{amb} = 70^\circ C$			50 100	μA μA
V_F	Clamp Diode Forward Voltage	$I_F = 1$ A $I_F = 1.5$ A			1.75 2	V V

SCHEMATIC DIAGRAM

ULN2074B : $R_{IN} = 350 \Omega$
 ULN2076B : $R_{IN} = 3 \text{ k}\Omega$

CTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for ULN2074B – ULN2076B $V_{CE} = 50 V$ $V_{CE} = 50 V$ $T_{amb} = 70^\circ C$			100 500	μA	1
$V_{(sus)}$	Collector-emitter Sustaining Voltage	for ULN2074B – ULN2076B $I_C = 100 mA$ $V_I = 0.4 V$	35			V	2
$V_{(sat)}$	Collector-emitter Saturation Voltage	$I_C = 500 mA$ $I_B = 625 \mu A$ $I_C = 750 mA$ $I_B = 935 \mu A$ $I_C = 1 A$ $I_B = 1.25 mA$ $I_C = 1.25 A$ $I_B = 2 mA$			1.1 1.2 1.3 1.4	V	3
$I_{(on)}$	Input Current	for ULN2074B $V_I = 2.4 V$ for ULN2074B $V_I = 3.75 V$ for ULN2076B $V_I = 5 V$ for ULN2076B $V_I = 12 V$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA	4
$V_{(on)}$	Input Voltage	for ULN2074B $V_{CE} = 2 V$ $I_C = 1 A$ $V_{CE} = 2 V$ $I_C = 1.5 A$ for ULN2076B $V_{CE} = 2 V$ $I_C = 1 A$ $V_{CE} = 2 V$ $I_C = 1.5 A$			2 2.5 6.5 10	V	5
t_{LH}	Turn-on Delay Time	0.5 V_I to 0.5 V_O			1	μs	
t_{HL}	Turn-off Delay Time	0.5 V_I to 0.5 V_O			1.5	μs	

CIRCUITS

Figure 1.

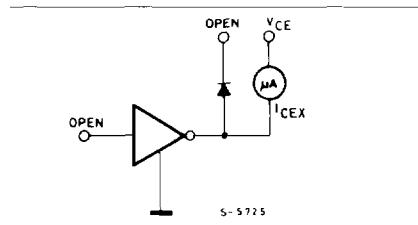


Figure 2.

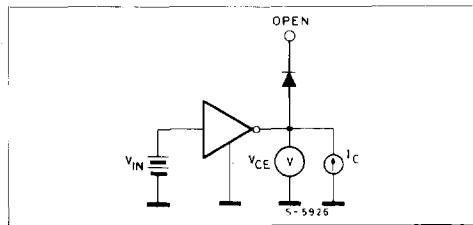


Figure 3.

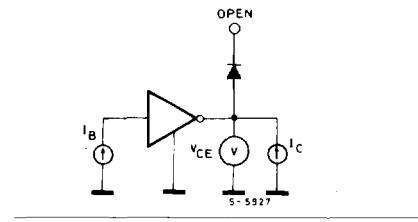


Figure 4.

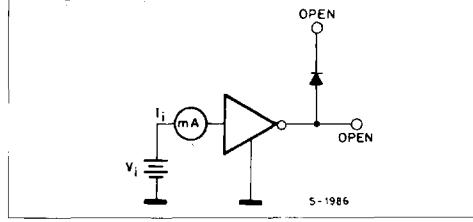


Figure 5.

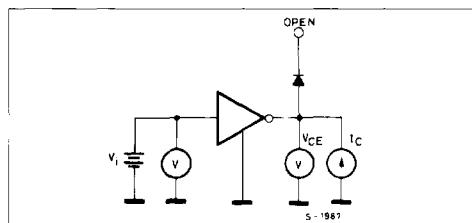


Figure 6.

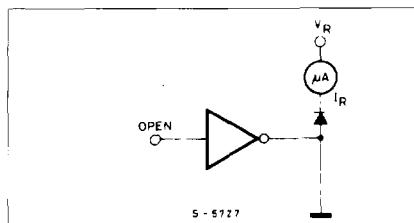


Figure 7.

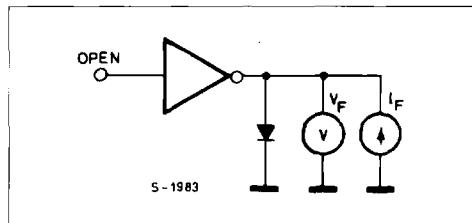


Figure 9 : Input Current as a Function of Input Voltage.

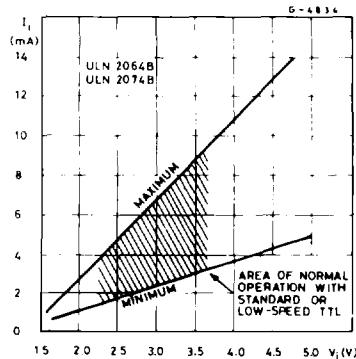


Figure 8.

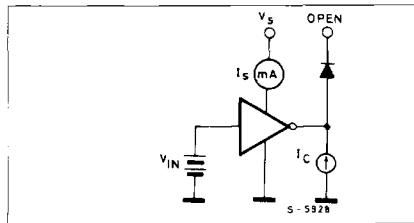


Figure 10 : Input Current as a Function of Input Voltage.

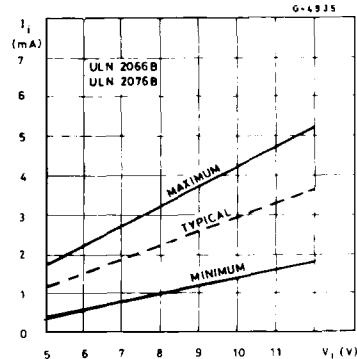
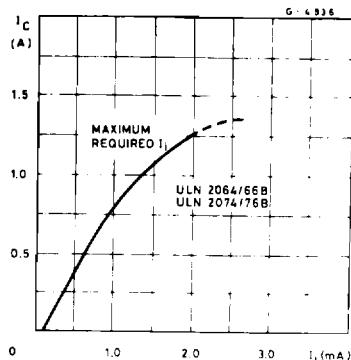


Figure 11 : Collector Current as a Function of Input Current.



CAL APPLICATIONS

Figure 12 : Common-anode LED Drivers.

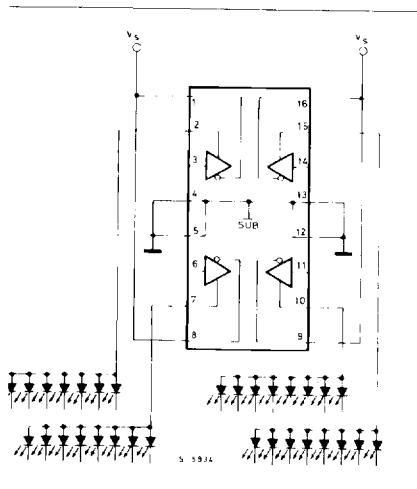
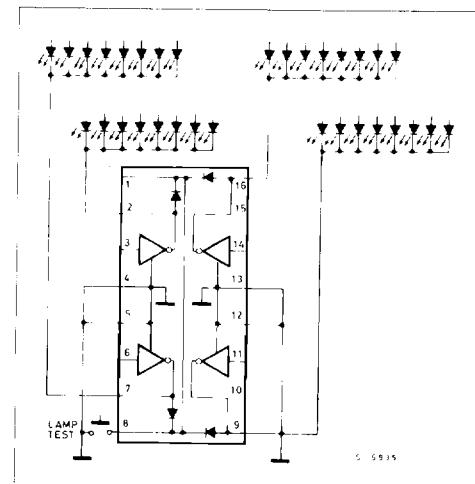


Figure 13 : Common-cathode LED Drivers.



MOUNTING INSTRUCTIONS

The $R_{th\ j\ -amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).

The diagram of figure 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\ -amb}$ as a function of the side "α" of two equal square copper areas having a thickness of 35μ (1.4 mils).

Figure 14 : Example of P.C. Board Copper Area which is Used as Heatsink.

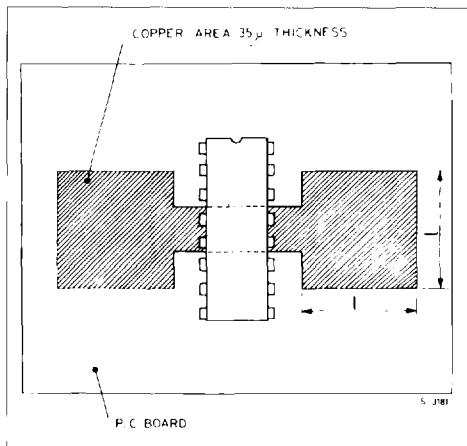
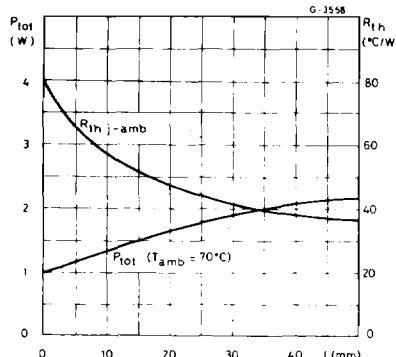


Figure 16 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "α".



During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper must be connected to electrical ground.

Figure 15 : External Heatsink Mounting Exam

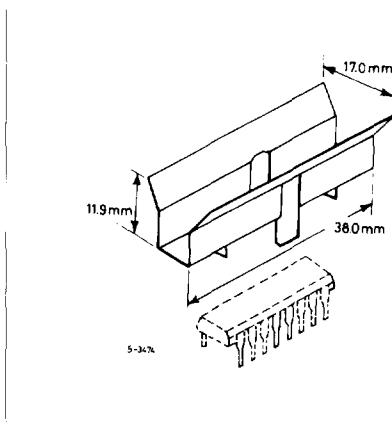


Figure 17 : Maximum Allowable Power Dissipation vs. Ambient Temperature

