

The SN74LS16 is obsolete and is no longer supplied.

# SN54LS06, SN74LS06, SN74LS16 HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

SDLS020D – MAY 1990 – REVISED FEBRUARY 2003

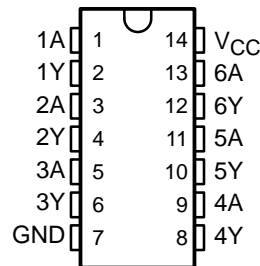
- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits

## description/ordering information

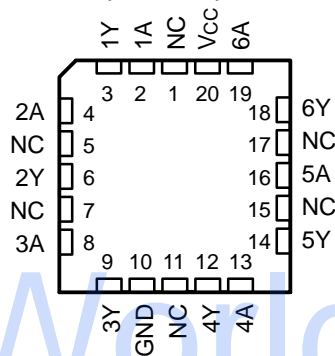
These hex inverter buffers/drivers feature high-voltage open-collector outputs to interface with high-level circuits (such as MOS), or for driving high-current loads, and also are characterized for use as inverter buffers for driving TTL inputs. The 'LS06 devices have a rated output voltage of 30 V, and the SN74LS16 has a rated output voltage of 15 V. The maximum sink current for the SN54LS06 is 30 mA, and for the SN74LS06 and SN74LS16 it is 40 mA.

These devices are compatible with most TTL families. Inputs are diode-clamped to minimize transmission effects, which simplifies design. Typical power dissipation is 175 mW, and average propagation delay time is 8 ns.

SN54LS06 . . . J PACKAGE  
SN74LS06, SN74LS16 . . . D, DB, N, OR NS PACKAGE  
(TOP VIEW)



SN54LS06 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

| TA             | PACKAGE†      |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|---------------|-----------------------|------------------|
| 0°C to 70°C    | PDIP – N      | Tube          | SN74LS06N             | SN74LS06N        |
|                | SOIC – D      | Tube          | SN74LS06D             | LS06             |
|                |               | Tape and reel | SN74LS06DR            |                  |
|                | SOP – NS      | Tape and reel | SN74LS06NSR           | 74LS06           |
| SSOP – DB      | Tape and reel | SN74LS06DBR   | LS06                  |                  |
| –55°C to 125°C | CDIP – J      | Tube          | SN54LS06J             | SN54LS06J        |
|                |               | Tube          | SNJ54LS06J            | SNJ54LS06J       |
|                | LCCC – FK     | Tube          | SNJ54LS06FK           | SNJ54LS06FK      |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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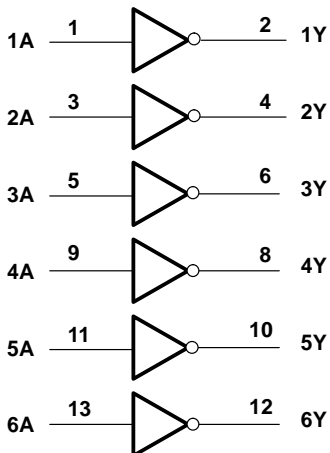
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54LS06, SN74LS06, SN74LS16 HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

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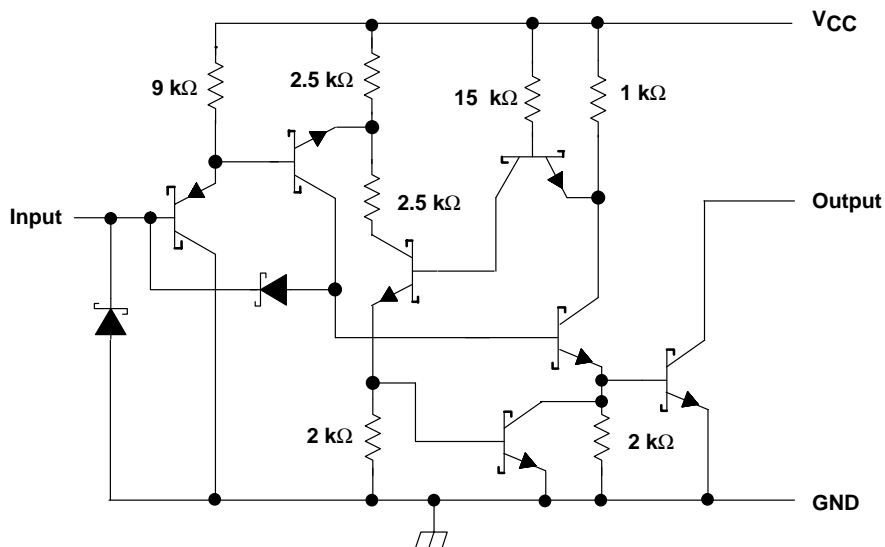
The SN74LS16 is obsolete  
and is no longer supplied.

## logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and NS packages.

## schematic (each gate)



Resistor values shown are nominal.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                |
|--|----------------|
| Supply voltage, $V_{CC}$   | 7 V            |
| Input voltage, $V_I$ (see Note 1)                                | 5.5 V          |
| Output voltage, $V_O$ (see Notes 1 and 2): SN54LS06, SN74LS06    | 30 V           |
| SN74LS16   | 15 V           |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): D package | 86°C/W         |
| DB package   | 96°C/W         |
| N package  | 80°C/W         |
| NS package   | 76°C/W         |
| Storage temperature range, $T_{stg}$                             | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.  
2. This is the maximum voltage that should be applied to any output when it is in the off state.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

|          |                                | SN54LS06 |     |     | SN74LS06<br>SN74LS16 |     |      | UNIT |
|----------|--------------------------------|----------|-----|-----|----------------------|-----|------|------|
|          |                                | MIN      | NOM | MAX | MIN                  | NOM | MAX  |      |
| $V_{CC}$ | Supply voltage                 | 4.5      | 5   | 5.5 | 4.75                 | 5   | 5.25 | V    |
| $V_{IH}$ | High-level input voltage       | 2        |     |     | 2                    |     |      | V    |
| $V_{IL}$ | Low-level input voltage        |          |     | 0.8 |                      |     | 0.8  | V    |
| $V_{OH}$ | High-level output voltage      | 'LS06    |     |     | 30                   |     |      | V    |
|          |                                | SN74LS16 |     |     | 15                   |     |      |      |
| $I_{OL}$ | Low-level output current       |          |     | 30  |                      |     | 40   | mA   |
| $T_A$    | Operating free-air temperature | -55      |     | 125 | 0                    |     | 70   | °C   |

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡                                 | SN54LS06                          |      |      | SN74LS06<br>SN74LS16 |      |      | UNIT |   |
|-----------|--|-----------------------------------|------|------|----------------------|------|------|------|---|
|           |  | MIN                               | TYP§ | MAX  | MIN                  | TYP§ | MAX  |      |   |
| $V_{IK}$  | $V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$   |                                   |      | -1.5 |                      |      | -1.5 | V    |   |
| $I_{OH}$  | $V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ | 'LS06, $V_{OH} = 30 \text{ V}$    |      |      | 0.25                 |      |      | mA   |   |
|           |  | SN74LS16, $V_{OH} = 15 \text{ V}$ |      |      | 0.25                 |      |      |      |   |
| $V_{OL}$  | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$   | $I_{OL} = 16 \text{ mA}$          |      |      | 0.25                 | 0.4  | 0.25 | 0.4  | V |
|           |  | $I_{OL} = 30 \text{ mA}$          |      |      | 0.7                  |      |      |      |   |
|           |  | $I_{OL} = 40 \text{ mA}$          |      |      | 0.7                  |      |      |      |   |
| $I_I$     | $V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$      |                                   |      | 1    |                      |      | 1    | mA   |   |
| $I_{IH}$  | $V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$    |                                   |      | 20   |                      |      | 20   | µA   |   |
| $I_{IL}$  | $V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$    |                                   |      | -0.2 |                      |      | -0.2 | mA   |   |
| $I_{CCH}$ | $V_{CC} = \text{MAX}$                            |                                   |      | 18   |                      |      | 18   | mA   |   |
| $I_{CCL}$ | $V_{CC} = \text{MAX}$                            |                                   |      | 60   |                      |      | 60   | mA   |   |

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^\circ\text{C}$ .



**SN54LS06, SN74LS06, SN74LS16**  
**HEX INVERTER BUFFERS/DRIVERS**  
**WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS**

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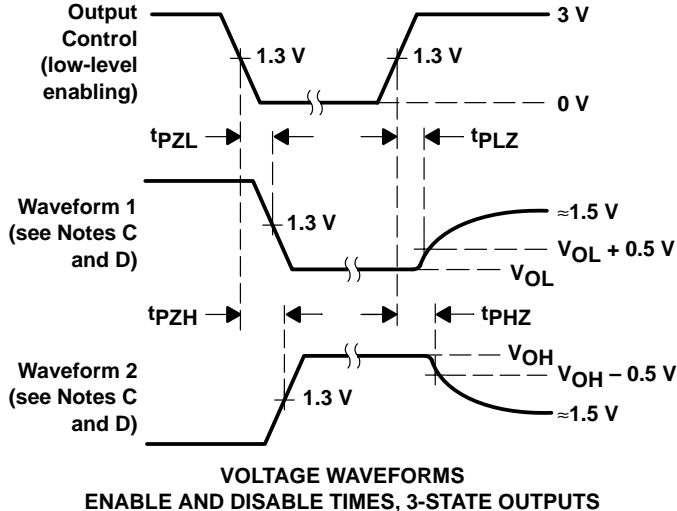
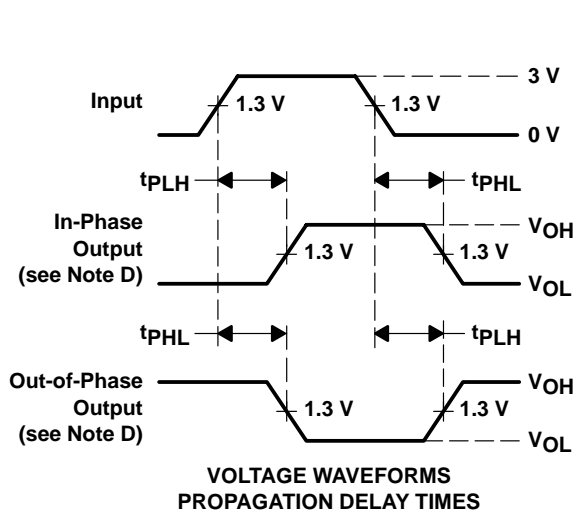
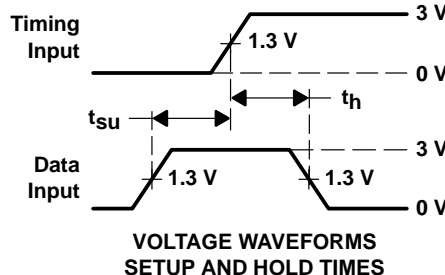
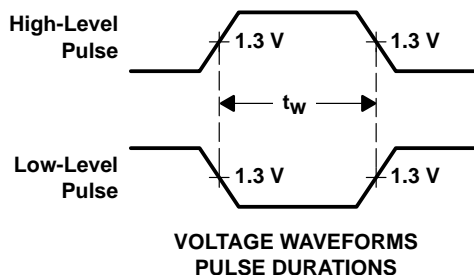
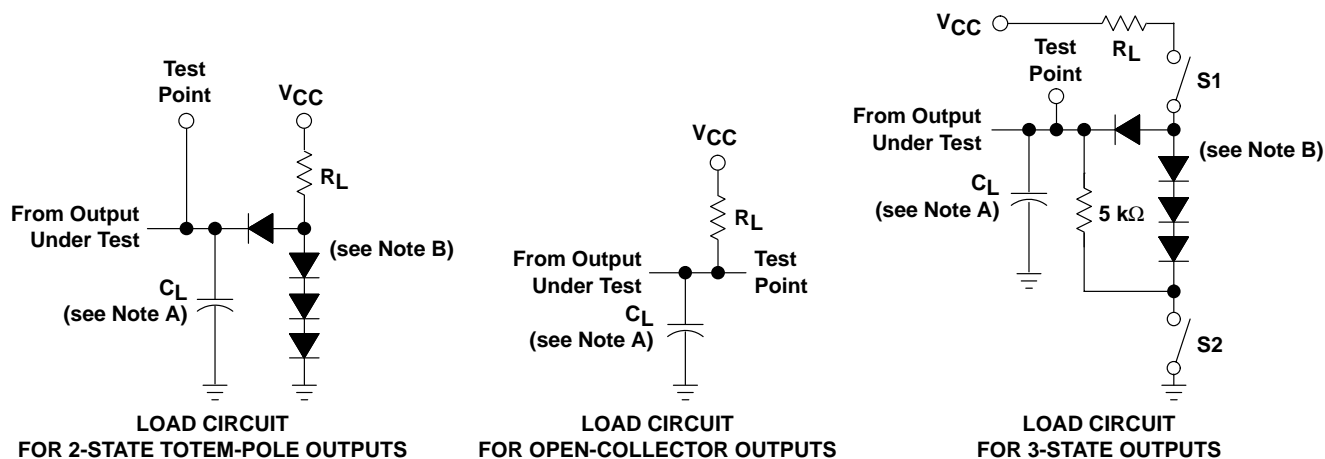
The SN74LS16 is obsolete  
and is no longer supplied.

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS                             | MIN | MAX | UNIT |
|-----------|--------------|-------------|---|-----|-----|------|
| $t_{PLH}$ | A            | Y           | $R_L = 110\ \Omega$ , $C_L = 15\ \text{pF}$ | 7   | 15  | ns   |
| $t_{PHL}$ |              |             |   | 10  | 20  |      |



PARAMETER MEASUREMENT INFORMATION



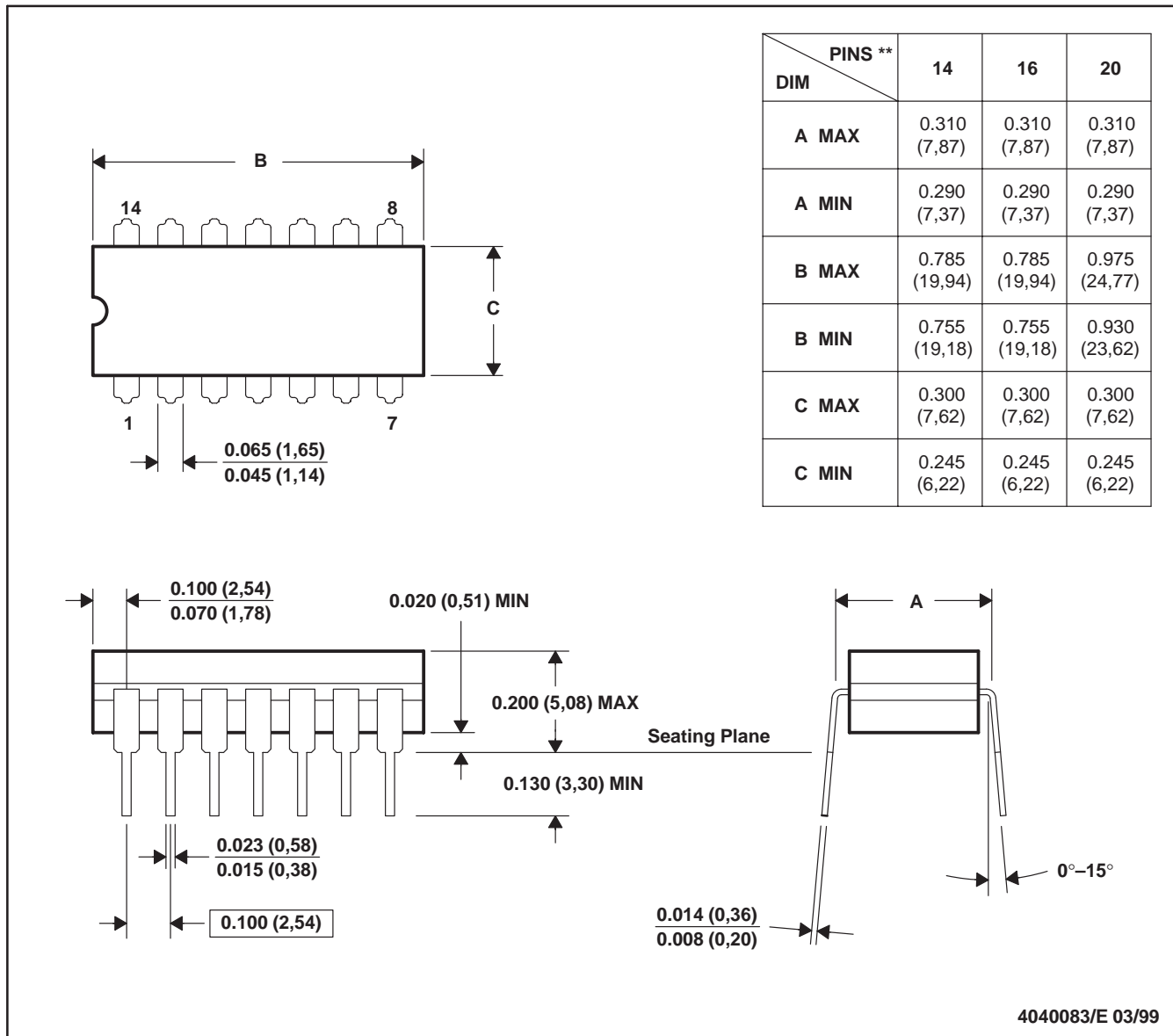
- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. All diodes are 1N3064 or equivalent.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .
  - E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
  - F. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 1.5$  ns,  $t_f \leq 2.6$  ns.
  - G. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

J (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

14 LEADS SHOWN

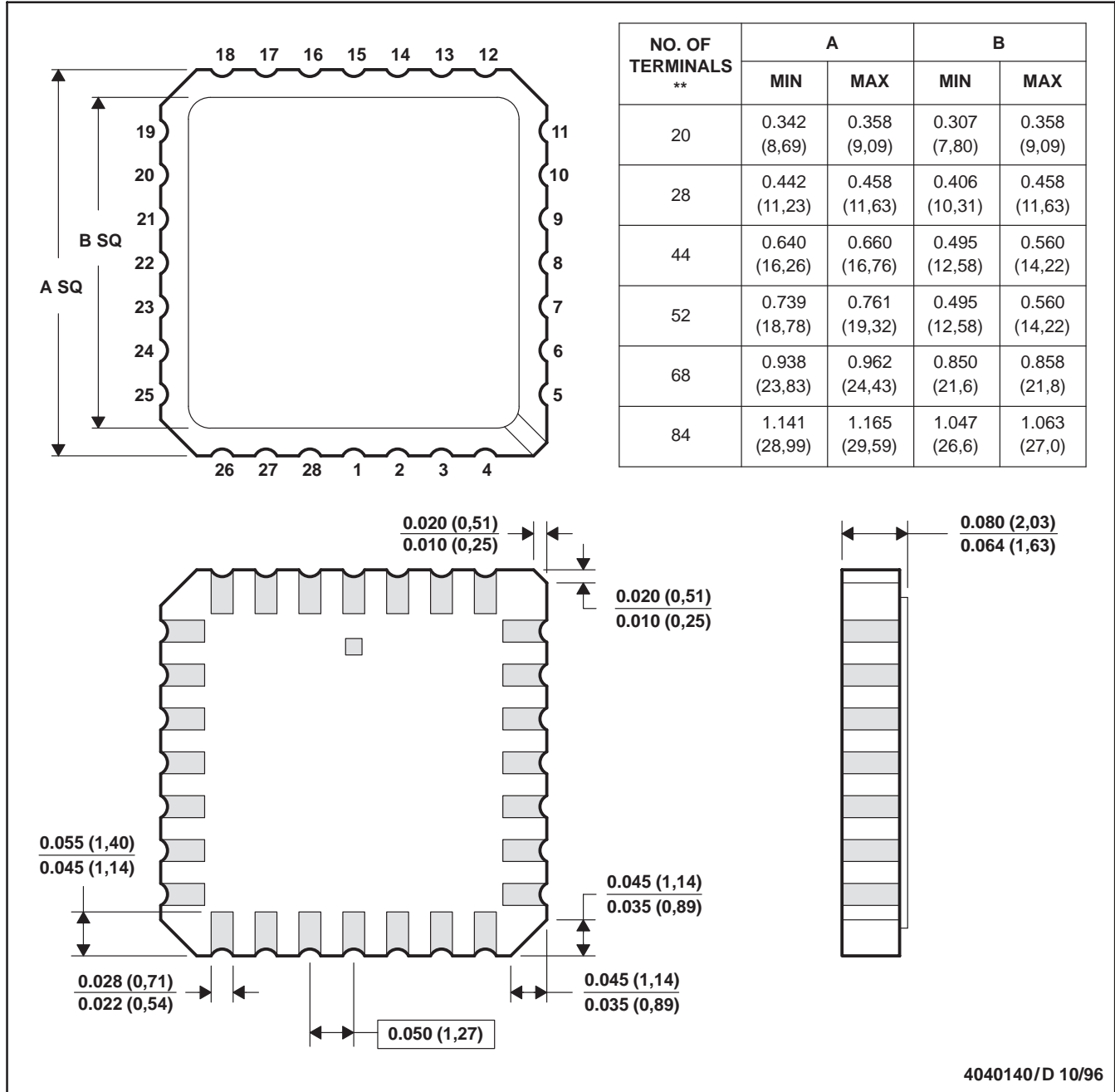


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package is hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, and GDIP1-T20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

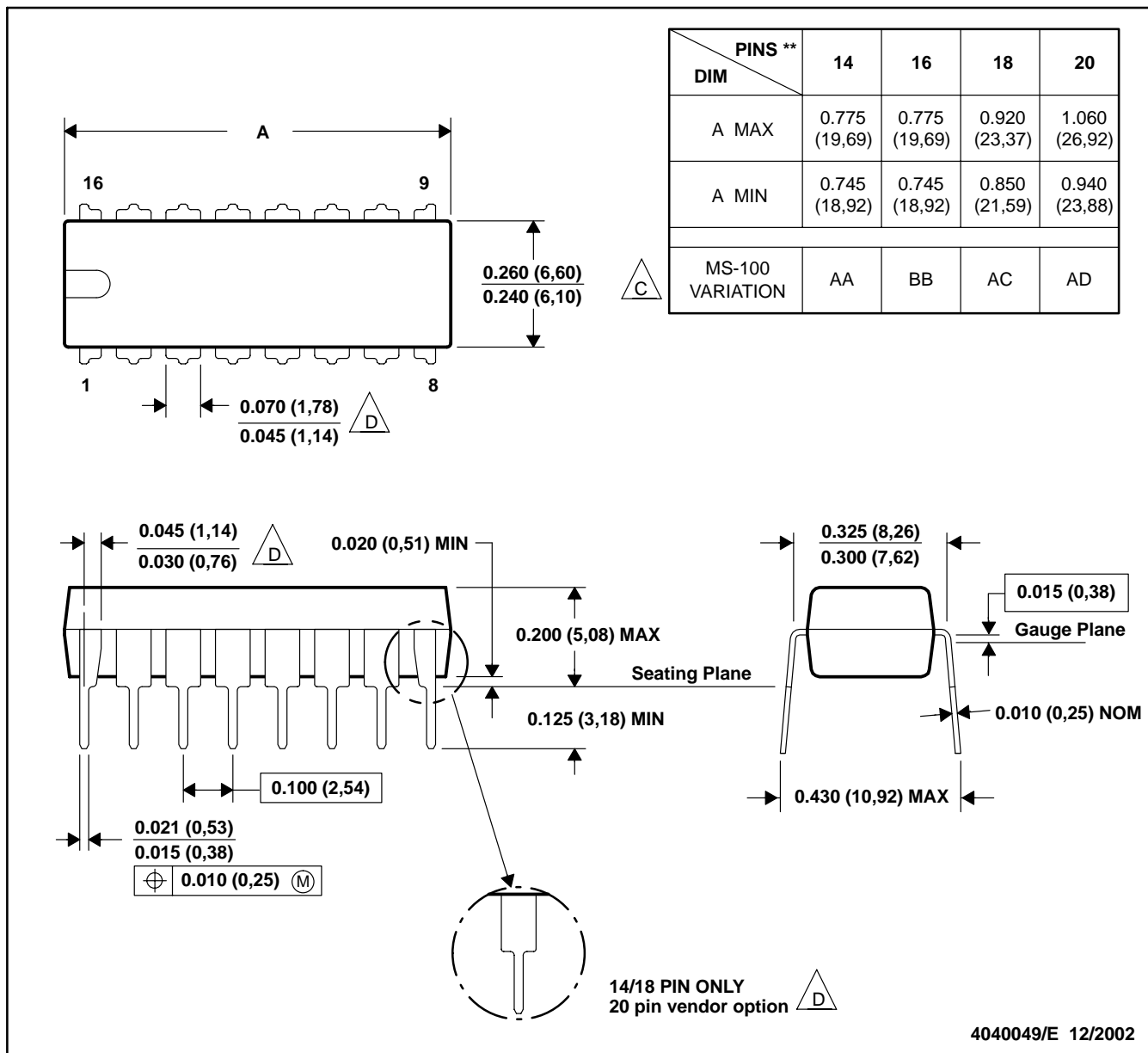


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



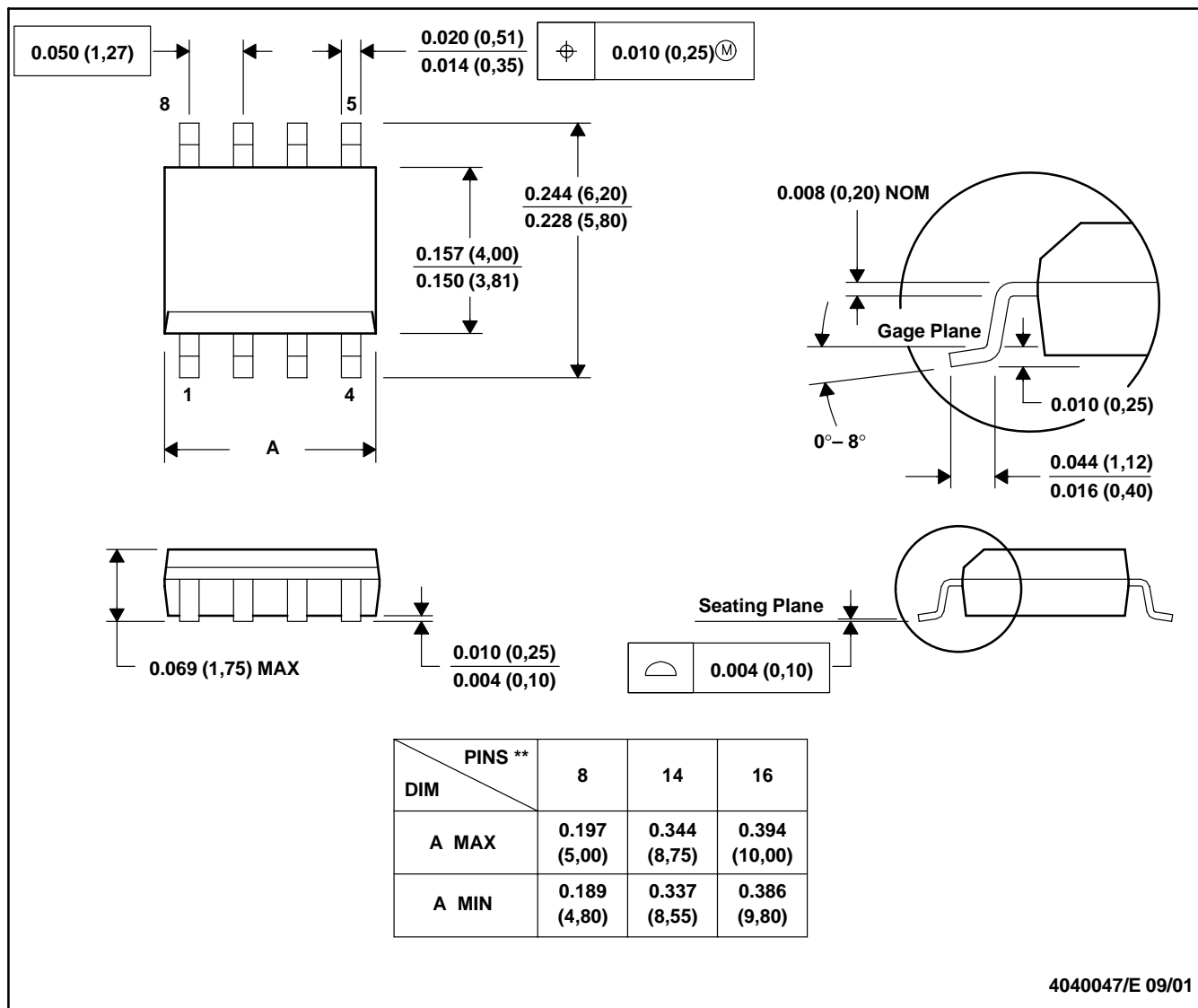
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

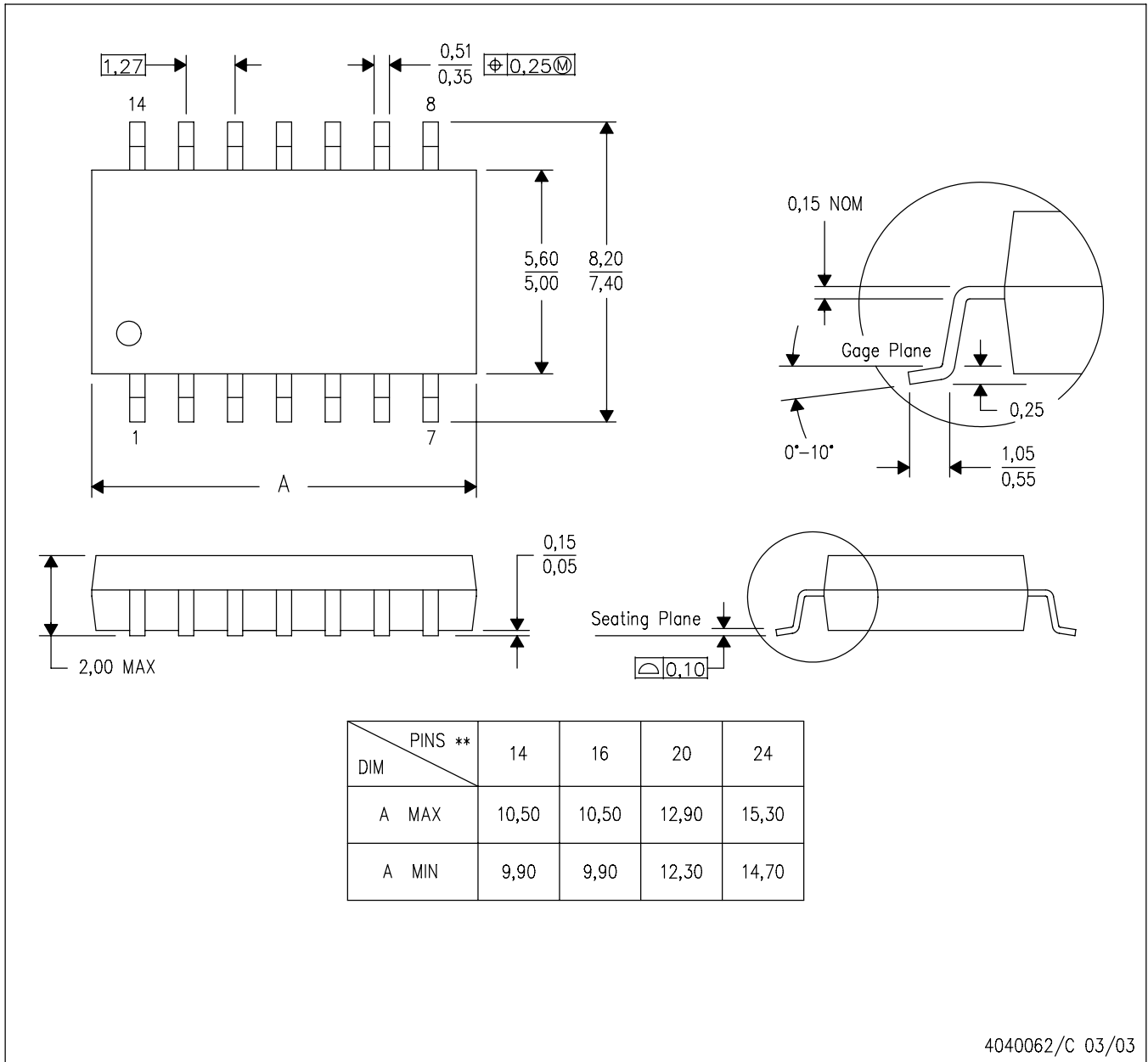
8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

NS (R-PDSO-G\*\*)  
14-PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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